SCHQ674401A-QF4060

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USB and DP Combo Linear Re-driver

1 Descriptions

SCHQ674401A-QF4060 is a USB 3.2 Gen 2 and DisplayPort 2.1 combo linear re-driver supporting data rates up to 10 Gbps. It integrates a cross point Mux for SBU signals rerouting. Both GPIO and I2C control methods are available for channel direction and equalization configuration.

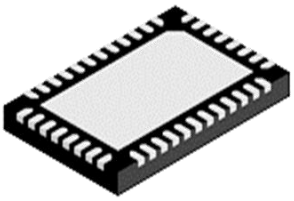

Figure 1 QFN4x6-40L (Bottom View)

2 Features

- USB / DP bi-directional combo linear re-driver
- Single 3.3 V ±10% power supply
- Supports USB-C USB and DisplayPort 2.1 Alt Mode application
- Cross-point Mux for SBU signals
- Configuration through GPIO or I2C for channel direction and equalization
- Auto power management for USB and DP links
- Supports signaling rates up to 10 Gbps
- -40°C to 85°C operating temperature
- QFN 4 mm x 6 mm 40-pin package

Y = Year code
W = Week code
UQ = Special code

Figure 2 Marking (Top View)

3 Applications

- Notebook, Desktop, and AIO PCs
- Tablet and Mobiles
- Docking and dongles

4 Order Information

Table 1 Order Information

Device	Package	Shipping
SCHQ674401A-QF4060	QFN4x6-40L	5000/ Tape&Reel

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5 Pin Configuration (Top View)

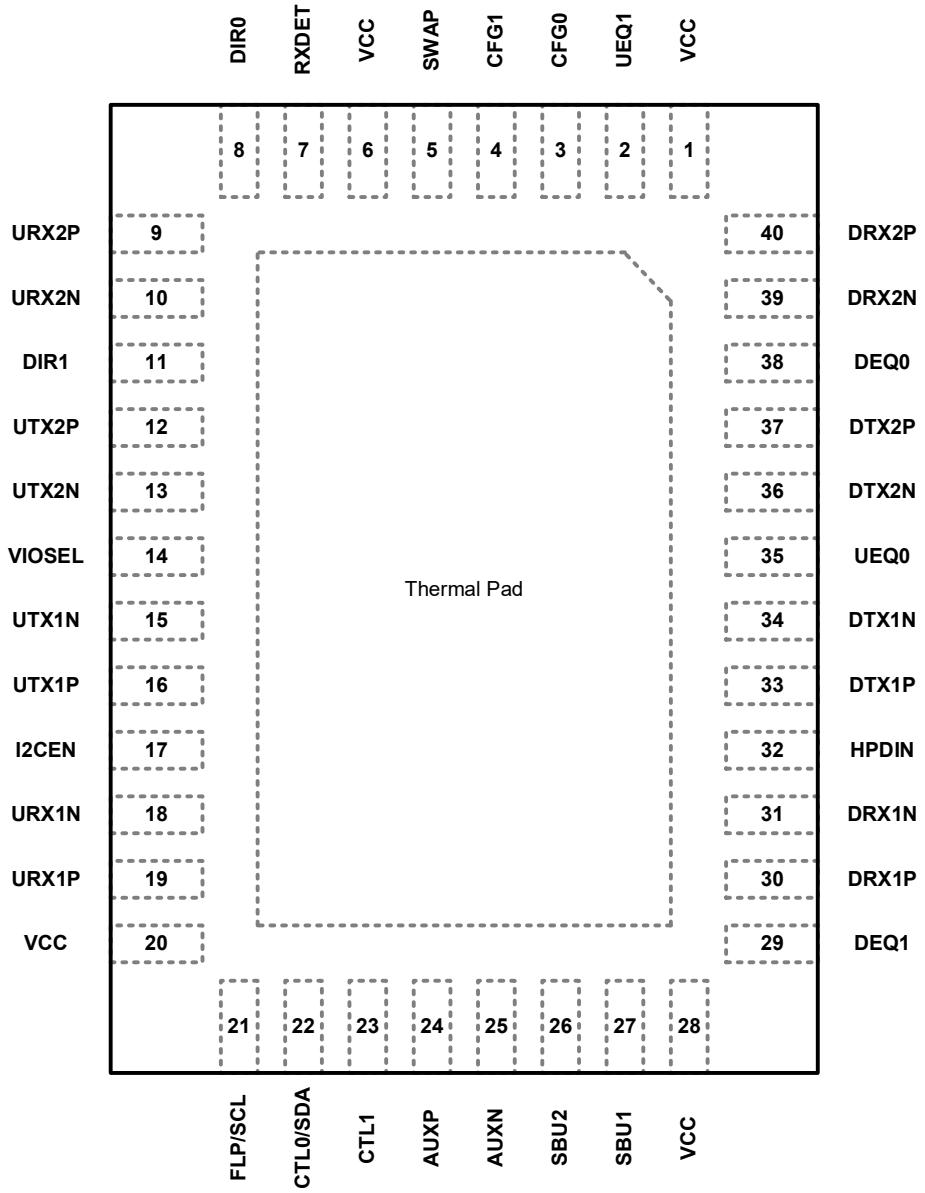


Figure 3 Pin Information (Top View)

Table 2 Pin Descriptions

Pin	Name	Type	Description
1, 6, 20, 28	VCC	Power	3.3 V power supply
2 35	UEQ1 UEQ0	4-Level Input	UEQ1_UEQ0 sets the EQ for upstream facing URX1/2, UTX1/2 receivers. In I2C Mode, this pin is used for I2C address configuration.
3 4	CFG0 CFG1	4-Level Input	CFG1_CFG0 sets VOD linearity range and DC gain for all the downstream and upstream channels.
5	SWAP	2-Level Input	Channel directions and EQ settings of data path inputs swapping. (Pulled-down internally) L: Do not swap; H: Swap.
7	RXDET	2-Level Input	Receiver detect function configuration. (Pulled-down internally) L: RX Detect disabled (U2/U3 state: disable LOS and LFPS detection, and keep RX termination on; No connection state: disable RX detection); H: RX Detect enabled.
8	DIR0	2-Level Input	Source/Sink side data path signal direction configuration. (Pulled-down internally) L: Source Side (DFP) Alt Mode; H: Sink Side (UFP) Alt Mode
9 10	URX2P URX2N	Diff I/O	Differential input/output for upstream facing RX2 port.
11	DIR1	2-Level I/O	Alternate Mode format configuration. (Pulled-down internally) L: DisplayPort Alt Mode; H: Custom Alt Mode format
12 13	UTX2P UTX2N	Diff I/O	Differential input/output for upstream facing TX2 port.
14	VIOSEL	4-Level I/O	2-level GPIO and I2C interface voltage level configuration: L: 3.3 V GPIO, 3.3 V I2C interface; R: 3.3 V GPIO, 1.8 V I2C interface; F: 1.8 V GPIO, 3.3 V I2C interface; H: 1.8 V GPIO, 1.8 V I2C interface;
15 16	UTX1N UTX1P	Diff I/O	Differential input/output for upstream facing TX1 port.
17	I2CEN	4-Level Input	I2C Mode or GPIO Mode configuration. L: GPIO Mode, AUX Snoop Enabled (I2C disabled). R: Test Mode (I2C enabled). F: GPIO Mode, AUX Snoop Disabled (I2C disabled). H: I2C enabled.
18 19	URX1N URX1P	Diff I/O	Differential input/output for upstream facing RX1 port.
21	FLIP/ SCL	2-Level Input	Flip control pin. (Pulled-down internally) In I2C Mode, I2C clock.
22	CTL0/ SDA	2-Level Input	USB3.1 Switch control pin. (Pulled-down internally) In I2C Mode, I2C data.
23	CTL1	2-Level Input	DP Alt mode Switch Control Pin. (GPIO Mode only, pulled-down internally) L: DisplayPort Disabled; H: DisplayPort Enabled.
24 25	AUXP AUXN	I/O, CMOS	DisplayPort AUX channel and AUX snooping source.

Pin	Name	Type	Description
26 27	SBU2 SBU1	I/O, CMOS	SBU2/1 pins of the Type-C receptacle reused for DisplayPort AUX channels.
29 38	DEQ1 DEQ0	4-Level Input	DEQ1_DEQ0 sets the EQ for downstream facing DRX1/2, DTX1/2 receivers.
30 31	DRX1P DRX1N	Diff I/O	Differential input/output for downstream facing RX1 port.
32	HPDIN	2-Level Input	Hot Plug Detection signal from DisplayPort sink. (Pulled-down internally) L: lasting for 2 ms, all DisplayPort lanes are disabled. H: AUX snoop or registers DisplayPort lanes enable is active.
33 34	DTX1P DTX1N	Diff I/O	Differential input/output for downstream facing TX1 port.
36 37	DTX2N DTX2P	Diff I/O	Differential input/output for downstream facing TX2 port.
39 40	DRX2N DRX2P	Diff I/O	Differential input/output for downstream facing RX2 port.
-	Thermal Pad	GND	Ground.

6 Block Diagrams

6.1 Application Block Diagram

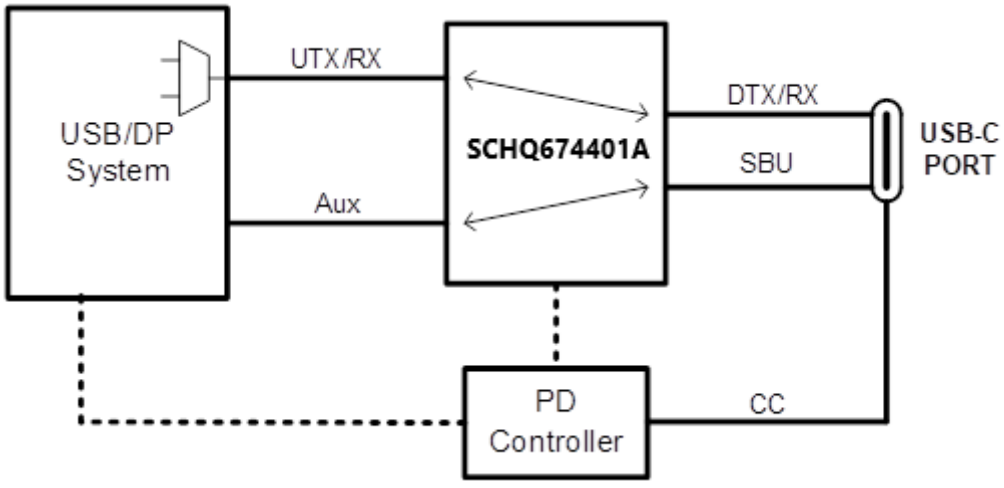


Figure 4 Application Information

6.2 Functional Block Diagram

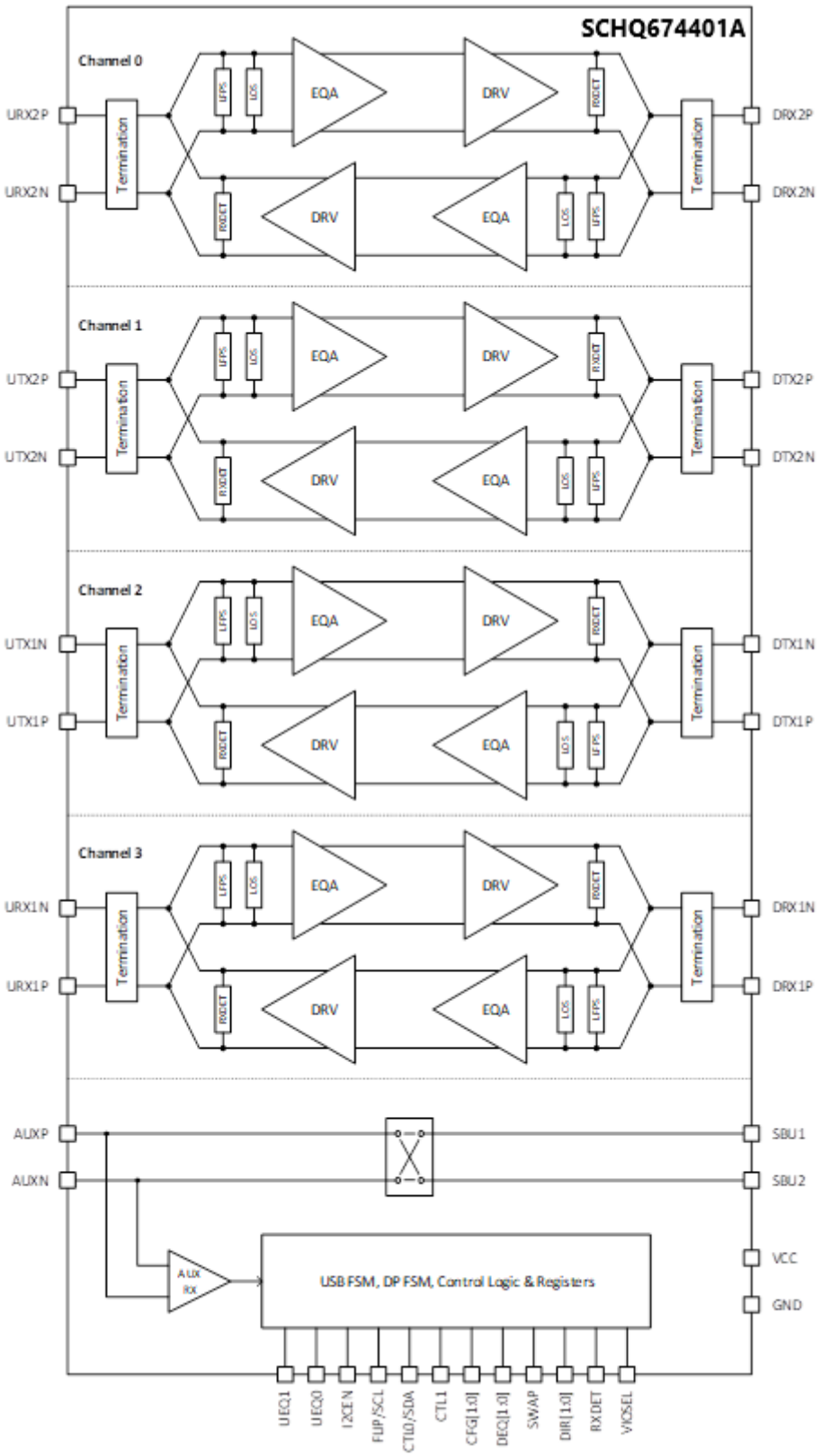


Figure 5 Functional Block Diagram

7 Specifications

7.1 Absolute Maximum Ratings

Maximum ratings are absolute ratings. Stresses exceeding any value in Table 3 might cause irreversible damage to the integrated circuit. Operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied.

Table 3 Absolute Maximum Ratings

Parameter	Symbol	Condition	Min.	Max.	Unit
Supply voltage range	V_{CC}	-	-0.3	4	V
Differential voltage at differential input pins	V_{IN_DIFF}	-	-	±2.5	V
Single-ended input voltage at differential input pins	V_{IN_SE}	-	-0.5	4	V
Input voltage at CMOS inputs	V_{IN_CMOS}	-	-0.3	4	V
Storage temperature	T_{stg}	-	-65	150	°C
ESD	V_{HBM}	ESDA/JEDEC JS-001-2017	±4		kV
	V_{CDM}	ESDA/JEDEC JS -002-2018	±1		kV
Moisture sensitivity	MSL	-	Level 3		

7.2 Recommended Operation Conditions

Recommended operation conditions define the conditions for actual device operation. Recommended operation conditions are specified to ensure optimal performance. WillSemi does not recommend exceeding the range or designing to values in Absolute Maximum Ratings.

Table 4 Recommended Operation Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	-	3.0	3.3	3.6	V
SDA and SCL pulled-up power voltage	V_{I2C}	-	1.7	-	3.6	V
Ambient temperature	T_A	-	-40	-	85	°C
Junction temperature	T_J	-	-	-	125	°C

7.3 Electrical Characteristics

V_{CC} = 3.0 V to 3.6 V, Ta = 25˚C, unless otherwise noted.

Table 5 Power and Latency

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Average power for USB 3.2 only mode	$P_{USB-ACTIVE}$	Link active with USB 3.2 GEN 2 data transmission	-	300	-	mW
Average power for USB 3.2 and 2-lane DP	$P_{USB-DP-ACTIVE}$	Link active with USB 3.2 GEN 2 data transmission and DP active	-	570	-	mW
Average power for USB 3.2 and 2-channel custom alt mode	$P_{CUSTOM-ACTIVE}$	Link active with USB 3.2 GEN 2 data transmission and custom alt mode active	-	570	-	mW
Average power for 4-lane DP	$P_{4DP-ACTIVE}$	Link active with 4-lane DP data transmission	-	530	-	mW
Average power for USB3.1 only and nothing connected	P_{USB-NC}	Nothing connected	-	0.85	-	mW
Average power for USB3.1 only and link in U2/U3 state	$P_{USB-U2U3}$	-	-	1.3	-	mW
Shutdown power	$P_{SHUTDOWN}$	-	-	0.45	-	mW

Table 6 4-State CMOS Inputs (UEQ[1:0];DEQ[1:0], CFG[1:0], A[1:0], I2CEN, VIOSEL)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High/Low-level input current during initialization for <1ms	I_{IH_INIT}	VCC = 3.6 V; VIN = 3.6 V	-	40	-	μA
	I_{IL_INIT}	VCC = 3.6 V; VIN = 0 V	-	-100	-	μA
High/Low-level input current during normal operation period	I_{IH}	VCC = 3.6 V; VIN = 3.6 V	-0.25	-	0.25	μA
	I_{IL}	VCC = 3.6 V; VIN = 0 V	-0.25	-	0.25	μA
Threshold L / Resistor (R)	4-Level V_{TH}	VCC = 3.3 V	-	0.55	-	V
Threshold R / Float (F)		VCC = 3.3 V	-	1.65	-	V
Threshold F / H		VCC = 3.3 V	-	2.7	-	V
Internal pull-up/down resistance during initialization for <1ms	R_{PU_INIT}	-	-	35	-	kΩ
	R_{PD_INIT}	-	-	95	-	kΩ
Internal pull-up/down resistance during normal operation period	R_{PU}	-	10	-	-	MΩ
	R_{PD}	-	10	-	-	MΩ

Table 7 2-State CMOS Input (CTL0, CTL1, FLIP, HPDIN, RXDET, SWAP, DIR[1:0])

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High-level input voltage	$V_{IH-3.3V}$	V_{CC} = 3.3V; VIOSEL = "L" or "R"	2	-	3.6	V
	$V_{IH-1.8V}$	V_{CC} = 3.3V; VIOSEL = "F" or "H"	1.2	-	3.6	V
Low-level input voltage	$V_{IL-3.3V}$	V_{CC} = 3.3V; VIOSEL = "L" or "R"	0	-	0.8	V
	$V_{IL-1.8V}$	V_{CC} = 3.3V; VIOSEL = "F" or "H"	0	-	0.4	V
Internal pull-down resistance	R_{PD}	CTL1, CTL0, DIR0, DIR1, FLIP, RXDET, HPDIN	-	460	-	kΩ

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
	R_{PD_SWAP}	SWAP	-	460	-	kΩ
High-level input current	I_{IH}	VIN = 3.6 V	-25	-	25	μA
Low-level input current	I_{IL}	VIN = GND, VCC = 3.6 V	-25	-	25	μA

Table 8 I2C Control Pins SCL, SDA

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High-level input voltage	$V_{IH-3.3V}$	V_{CC} = 3.3V; VIOSEL = "L" or "F";	2	-	3.6	V
	$V_{IH-1.8V}$	V_{CC} = 3.3V; VIOSEL = "R" or "H";	1.2	-	3.6	V
Low-level input voltage	$V_{IL-3.3V}$	V_{CC} = 3.3V; VIOSEL = "L" or "F";	0	-	0.8	V
	$V_{IL-1.8V}$	V_{CC} = 3.3V; VIOSEL = "R" or "H";	0	-	0.4	V
Low-level output voltage	V_{OL}	I_{OL} = 3 mA	0	-	0.4	V
Low-level output current	I_{OL}	V_{OL} = 0.4 V	20	-	-	mA
Input current on SDA pin	I_{I_I2C}	0.1*V_{I2C} < Input voltage < 3.3 V	-15	-	15	μA
Input capacitance	C_{I_I2C}	-	0.5	-	5	pF

Table 9 USB Gen 2 Differential Receiver (UTX1P/N, UTX2P/N, DRX1P/N, DRX2P/N)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input differential peak-to-peak voltage swing dynamic range	$V_{RX-DIFF-PP}$	AC-coupled differential peak-to-peak signal	-	1800	-	mV_{pp}
RX common-mode bias voltage	$V_{RX-DC-CM}$	-	-	0	-	V
Differential input impedance	$R_{RX-DIFF-DC}$	RX is detected	72	-	120	Ω
Common mode input impedance	$R_{RX-CM-DC}$	RX is detected	18	-	30	Ω
Input impedance during no connection	$Z_{RX-HIGH-IMP-DC-POS}$	No RX is detected	25	-	-	kΩ
Input differential peak-to-peak signal detect assert level	$V_{SIGNAL-DET-DIFF-PP}$	-	-	80	-	mV
Input differential peak-to-peak signal detect de-assert level	$V_{RX-IDLE-DET-DIFF-PP}$	-	-	80	-	mV
LFPS detection threshold	$V_{RX-LFPS-DET-DIFF-PP}$	-	100	-	300	mV
Differential return loss	$RL_{RX-DIFF}$	-	-	-14	-	dB
Common mode return loss	RL_{RX-CM}	-	-	-10	-	dB
Maximum receiver equalization setting	EQ_{SSP}	at 5 GHz	-	10.1	-	dB

Table 10 USB Gen 2 Differential Transmitter (DTX1P/N, DTX2P/N, URX1P/N, URX2P/N)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmitter differential voltage swing dynamic range	$V_{TX-DIFF-PP}$	-	-	1400	-	mV_{pp}
Amount of voltage change during receiver detection	$V_{TX-RCV-DETECT}$	-	-	-	600	mV
Transmitter idle common-mode voltage change while in U2/U3 and not actively transmitting LFPS	$V_{TX-CM-IDLE-DELTA}$	-	-600	-	600	mV
TX common-mode voltage bias voltage	$V_{TX-DC-CM}$	-	-	1.9	-	V
AC electrical idle differential peak-to-peak output voltage	$V_{TX-IDLE-DIFF-AC-PP}$	-	0	-	10	mV
DC Electrical idle differential output voltage	$V_{TX-IDLE-DIFF-DC}$	-	0	-	14	mV
TX differential impedance	$R_{TX-DIFF}$	-	75	-	120	Ω
AC coupling capacitor	C_{AC}	-	75	-	265	nF
TX common-mode impedance	R_{TX-CM}	-	18	-	30	Ω
TX short circuit current	$I_{TX-SHORT}$	-	-	-	74	mA
Differential return loss	$RL_{TX-DIFF}$	-	-	-15	-	dB
Common mode return loss	RL_{TX-CM}	-	-	-10	-	dB

Table 11 AC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Differential crosstalk	Crosstalk	At 5 GHz	-	-30	-	dB
Low-frequency voltage gain	G_{LF}	At 100 MHz; 0 dB DC gain	-1	0	1	dB
Low-frequency -1dB compression point	$CP_{1dB-LF-1100}$	At 100 MHz; 1100mVpp linearity	-	1150	-	mV_{pp}
High-frequency -1dB compression point	$CP_{1dB-HF-1100}$	At 5 GHz; 1100mVpp linearity setting;	-	1050	-	mV_{pp}
Low-frequency cutoff	f_{LF}	-	-	22	50	kHz
TX output deterministic jitter	D_J	-	-	0.07	-	UIpp
TX output total jitter	T_J	-	-	0.11	-	UIpp

Table 12 DisplayPort Receiver (UTX1P/N, UTX2P/N, URX1P/N, URX2P/N)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input differential peak-to-peak voltage swing dynamic range	V_{ID_PP}	-	-	1500	-	mV
AC coupling capacitance	C_{AC}	-	75	-	265	nF
Maximum receiver equalization setting	EQ_{DP}	at 4.05 GHz	-	10.2	-	dB
Data rate supported	d_R	-	-	10	-	Gbps
Differential input impedance	R_{ti}	-	80	100	120	Ω

Table 13 DisplayPort Transmitter (DTX1P/N, DTX2P/N, DRX1P/N, DRX2P/N)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
VOD dynamic range	$V_{TX\text{-}DIFFPP}$	-	-	1500	-	mV

Table 14 AUXP/N and SBU1/2

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
ON resistance	R_{ON}	V_{CC} = 3.3 V; V_I = 0 to 0.4 V for AUXP; V_I = 2.7 V to 3.6 V for AUXN	-	5.5	10	Ω
ON resistance mismatch	ΔR_{ON}	V_{CC} = 3.3 V;	-	-	1	Ω
ON resistance flatness	R_{ON_FLAT}	V_{CC} = 3.3 V;	-	-	2	Ω
DC common mode voltage for AUXP and SBU1.	$V_{AUXP\_DC\_CM}$	V_{CC} = 3.3 V	0	-	0.4	V
DC common mode voltage for AUXN and SBU2	$V_{AUXN\_DC\_CM}$	V_{CC} = 3.3 V	2.7	-	3.6	V

7.4 Switching Characteristics

Table 15 USB 3.2

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Delay for LFPS pattern	t_{IDLE_LFPS}	-	-	0.16	-	ns
U2/U3 exit time	$t_{IDLE\_Exit\_U2U3}$	-	-	5	-	μs
RX detect interval	t_{RXDET_INTVL}	-	-	-	12	ms
Disconnect exit time	$t_{IDLE\_Exit\_DISC}$	-	-	12	-	ms
Shutdown exit time	t_{Exit_SHTDN}	-	-	0.5	-	ms
Differential propagation delay	t_{DIFF_DLY}	-	-	-	300	ps
Power up time	$t_{PWR\_UP\_ACTIVE}$	From 70% Vcc to device active	-	-	1	ms

7.5 Timing Requirements

Table 16 I2C Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
I2C clock frequency	f_{SCL}	-	-	1	MHz
Hold time after repeated START condition. After this period, the first clock pulse is generated	t_{HDSTA}	0.26	-	-	μs
Low period of the I2C clock	t_{LOW}	0.5	-	-	μs
High period of the I2C clock	t_{HIGH}	0.26	-	-	μs
Setup time for a repeated START condition	t_{SUSTA}	0.26	-	-	μs
Data hold time	t_{HDDAT}	0	-	-	μs
Data setup time	t_{SUDAT}	50	-	-	ns
Rise time of both SDA and SCL signals	t_R	-	-	120	ns
Fall time of both SDA and SCL signals	t_F	20 × (V_{I2C}/5.5V)	-	120	ns
Setup time for STOP condition	t_{SUSTO}	0.26	-	-	μs
Bus free time between START and STOP conditions	t_{BUF}	0.5	-	-	μs

Table 17 HPDIN

Parameter	Symbol	Min.	Typ.	Max.	Unit
HPDIN debounce time for transitioning from H to L	$t_{CTL1\_DEBOUNCE}$	2.5	-	-	ms

Table 18 USB3.1 and DisplayPort mode transition requirement in GPIO mode

Parameter	Symbol	Min.	Typ.	Max.	Unit
Minimum overlap of CTL0 and CTL1 when transitioning from USB 3.2 only mode to 4-Lane DisplayPort mode or vice versa	$t_{GP\_USB\_4DP}$	4	-	-	μs

Table 19 Power-on timings

Parameter	Symbol	Min.	Typ.	Max.	Unit
CFG pins setup time	t_{cfg_su}	350	-	-	μs
CFG pin hold time	t_{cfg_hd}	10	-	-	μs
CTL[1:0] and FLIP pin debounce	t_{ctl_db}	-	-	16	ms
VCC supply ramp up	t_{VCC_RAMP}	0.1	-	100	ms

8 Function Description

8.1 Overview

The SCHQ674401A is a USB Type-C Alt Mode re-driver switch that supports data rates up to 10 Gbps. It is designed for use with configurations C, D, E, and F from the VESA DisplayPort Alt Mode on USB Type-C Standard, and can also be configured to support custom USB Type-C alternate modes.

The SCHQ674401A offers multiple levels of receive equalization to offset the effects of inter-symbol interference (ISI) caused by cable and board trace loss when USB 3.2 Gen 2 or DisplayPort (or other Alt modes) signals travel over a PCB or cable. This device requires a 3.3V power supply and is available for operation in both commercial and industrial temperature ranges.

The SCHQ674401A can enable host (source) or device (sink) applications to pass transmitter compliance and receiver jitter tolerance tests for USB 3.2 Gen 2 and DisplayPort version 2.1 UHBR10. This is accomplished through the re-driver's ability to recover incoming data by applying equalization that compensates for channel loss, and driving out signals with a high differential voltage.

- Each channel has a receiver equalizer with selectable gain settings, and equalization control for upstream and downstream facing ports can be set using UEQ[1:0] and DEQ[1:0] pins respectively, or through the I2C interface.

The SCHQ674401A offers the flexibility to adjust the EQ DC gain and voltage linearity range for all channels using the CFG[1:0] pins or equivalent I2C registers (refer to **Table 27**). This level of control simplifies the process of configuring the device to meet various standard compliance requirements.

The SCHQ674401A incorporates an advanced state machine that enables it to operate transparently with hosts and devices. Upon power-up, the SCHQ674401A periodically performs receiver detection on the TX pairs, and if a USB 3.2 receiver is detected, the RX termination is enabled, and the SCHQ674401A is ready to re-drive.

The device provides highly flexible data path signal direction control through the CTL[1:0], FLIP, DIR[1:0], and SWAP pins or through the I2C interface. **Table 23** provides detailed information on the input to output signal pin mapping.

With an ultra-low-power architecture that operates at a 3.3 V power supply, the SCHQ674401A achieves enhanced performance. Additionally, the device's automatic LFPS De-Emphasis control enables the system to comply with USB 3.2 requirements.

8.2 Feature Description

8.2.1 USB 3.2

The SCHQ674401A supports USB 3.2 data rates up to 10 Gbps and all USB-defined power states, including U0, U1, U2, and U3. However, since it is a linear re-driver, it cannot decode USB3.1 physical layer traffic. Instead, it relies on monitoring the physical layer conditions such as receiver termination, electrical idle, LFPS, and SuperSpeed signaling rate to determine the USB power state of the USB3.1 interface.

The SCHQ674401A is equipped with an intelligent low frequency periodic signaling (LFPS) detector that automatically senses low frequency signals and disables receiver equalization functionality. The device enables receiver equalization based on the UEQ[1:0] and DEQ[1:0] pins or values programmed into UEQ[3:0]_SEL and DEQ[3:0]_SEL registers when not receiving LFPS.

8.2.2 DisplayPort

The SCHQ674401A supports up to 4 DisplayPort lanes with data rates up to 10 Gbps (UHBR10). When operating in DisplayPort mode, the SCHQ674401A monitors the native AUX traffic as it flows between DisplayPort source and DisplayPort sink. In order to conserve power, the SCHQ674401A manages the number of active DisplayPort lanes based on the contents of the AUX transactions. Specifically, the SCHQ674401A snoops native AUX writes to the DisplayPort sink's DPCD registers 00101h (LANE_COUNT_SET) and 00600h (SET_POWER_STATE). If a value is written to LANE_COUNT_SET, the SCHQ674401A will enable or disable lanes accordingly. If SET_POWER_STATE is in the D3 state, all lanes will be disabled. Otherwise, the number of active lanes will be based on the value of LANE_COUNT_SET.

DisplayPort AUX snooping is enabled by default, but it can be disabled by changing the AUX_SNOOP_DISABLE register. Once AUX snoop is disabled, the management of SCHQ674401A DisplayPort lanes will be controlled through various configuration registers.

8.2.3 4-level Control Pins

The SCHQ674401A features 4-level input pins (I2C_EN, UEQ[1:0], DEQ[1:0], CFG[1:0], and A[1:0]) which are utilized to regulate the equalization gain, voltage linearity range, and operating modes of the device. The resistor divider is employed to establish the 4 valid levels and provide a broader range of control settings for these inputs. Both an internal pull-up and pull-down resistor are integrated, along with the external resistor connection, to achieve the desired voltage level.

Table 20 4-level control pin settings

Level	Mapping
0 (L)	Pull-down (to GND) by 1 kΩ(5%) or 0Ω
R	Pull-down by 20kΩ (5%)
F	Open (Floating)
1 (H)	Pull-up (to V_{CC}) by 1 kΩ (5%) or 0Ω

Note: All four-level inputs of the SCHQ674401A are captured by a latch on the rising edge of the internal reset signal. Following the completion of t_{cfg_hd}, the internal pull-up and pull-down resistors are disabled to save power.

8.2.4 Receiver Linear Equalization

The receiver equalization aims to compensate for the channel insertion loss and inter-symbol interference in the system. The receiver mitigates these losses by attenuating the low-frequency components of the signal relative to the high-frequency components.

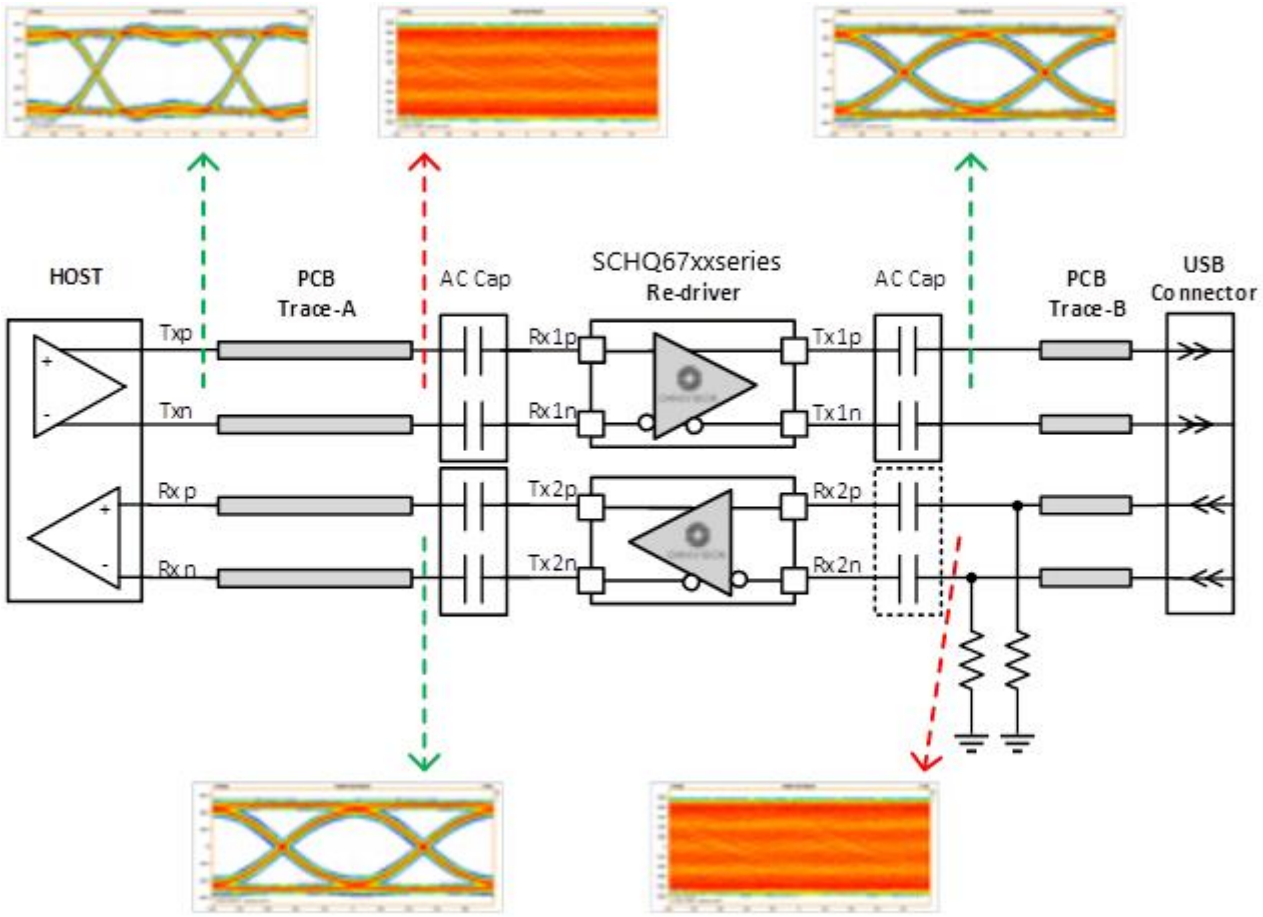


Figure 6 Typical Function and Application of Re-driver

The appropriate gain setting should be selected to match the channel insertion loss. Two 4-level input pins, UEQ[1:0] and DEQ[1:0], enable up to 16 possible equalization settings, with each upstream path and downstream path having their own. Additionally, the SCHQ674401A provides flexibility in adjusting equalization settings for each individual channel and for each direction (upstream or downstream) through I2C registers URX[2:1]EQ_SEL, UTX[2:1]EQ_SEL, DRX[2:1]EQ_SEL, and DTX[2:1]EQ_SEL.

8.3 Functional Operations

8.3.1 DisplayPort Mode

The SCHQ674401A device has the capability to support up to four DisplayPort lanes at a maximum data rate of 10 Gbps. The DisplayPort functionality can be enabled through either GPIO control or I2C register control. When in GPIO mode, the DisplayPort operation is governed based on **Table 21**. However, if the device is not in GPIO mode, the activation of the DisplayPort functionality is controlled through the I2C registers.

8.3.2 Custom Alternate Mode

The SCHQ674401A has the capability to support up to two lanes (or 4 channels) of Custom Alternate Mode at data rate up to 10 Gbps. It can be enabled through either GPIO control or I2C register control. However, Custom Alternate mode is not supported for GPIO mode which has AUX snoop disabled. In GPIO mode, the control of Custom Alternate Mode is based on **Table 21**. On the other hand, in non-GPIO mode, the enablement of Custom Alternate Mode functionality is controlled via I2C registers. It is important to note that in I2C mode, the operation of this mode requires leaving the AUX_SNOOP_DISABLE register 13h bit 7 at 0.

8.3.3 Device Configuration in GPIO mode

When the value of I2C_EN is set to "0" or "F", the SCHQ674401A operates in GPIO configuration.

By configuring the DIR1 pin, the SCHQ674401A supports two operational combinations with USB and two different Type-C alternate modes, which are DP alternate mode and custom alternate mode.

When DIR1 = 0, the combination consists of USB and DP alternate mode;

When DIR1 = 1, the combination consists of USB and custom alternate mode.

The data path directions for each operational combination can be further configured using the DIR0 pin or through I2C to enable the device to operate as either a source or a sink.

When DIR0 = 0, the device is set to operate in the source side;

When DIR0 = 1, the device is set to operate in the sink side;

Table 21 provides details on the configuration of all operational modes.

When operating in a combination of USB and DP alternate mode, the SCHQ674401A allows for further configuration, including USB3.1 only, 2 DP lanes + USB3.1, and 4 DP lanes (without USB3.1). The CTL1 pin is used to enable DisplayPort mode, and the combination of CTL1 and CTL0 pins is used to select between USB3.1 only, 2 lanes of DisplayPort, or 4 lanes of DisplayPort, as described in **Table 21**. The mapping of AUXP/N to SBU1/2 is controlled according to the specifications listed in **Table 22**.When operating in a combination of USB and custom alternate mode, the SCHQ674401A allows for further configuration, including USB3.1 only, 2 channels of custom alternate mode + USB3.1, and 4 channels of custom alternate mode (without USB3.1). The CTL1 pin is used to enable custom alternate mode, and the combination of CTL1 and CTL0 pins is used to select between USB3.1 only, 2 channels of custom alternate mode, or 4 channels of custom alternate mode, as described in **Table 21**. The mapping of AUXP/N to SBU1/2 is controlled according to the specifications listed in **Table 22**.

The SWAP pin allows for further control of data path direction. When set high, the SWAP pin reverses the data path direction on all channels and swaps the equalization settings of the upstream and downstream facing input ports. This pin is useful in active cable applications where the SCHQ674401A is installed on only one end, and the SWAP pin can be set based on which cable end is plugged into the source or sink side receptacle.

Upon power-up (VCC from 0 V to 3.3 V), the SCHQ674401A defaults to USB3.1 mode. If the USB PD controller detects no device attached to the Type-C port or USB3.1 operation is not required by the attached device, it must take the SCHQ674401A out of USB3.1 mode by transitioning the CTL0 pin from low to high and back to low.

Table 21 GPIO configuration – device mode control

DIR1	DIR0	CTL1	CTL0	FLIP	Device Configuration	VESA DP Alt Mode DFP_D Configuration
USB + DP alternate mode (Source side)						
L	L	L	L	L	Power Down	-
L	L	L	L	H	Power Down	-
L	L	L	H	L	1-port USB 3.2	-
L	L	L	H	H	1-port USB 3.2 with Flip	-
L	L	H	L	L	4-lane DP	C and E
L	L	H	L	H	4-lane DP with Flip	C and E
L	L	H	H	L	1-port USB 3.2 + 2-lane DP	D and F
L	L	H	H	H	1-port USB 3.2 + 2-lane DP with Flip	D and F
USB + DP alternate mode (Sink side)						
L	H	L	L	L	Power Down	-
L	H	L	L	H	Power Down	-
L	H	L	H	L	1-port USB 3.2	-
L	H	L	H	H	1-port USB 3.2 with Flip	-
L	H	H	L	L	4-lane DP	C and E
L	H	H	L	H	4-lane DP with Flip	C and E
L	H	H	H	L	1-port USB 3.2 + 2-lane DP	D and F
L	H	H	H	H	1-port USB 3.2 + 2-lane DP with Flip	D and F
USB + Custom alternate mode (Source side)						
H	L	L	L	L	Power Down	-
H	L	L	L	H	Power Down	-
H	L	L	H	L	1-port USB 3.2	-
H	L	L	H	H	1-port USB 3.2 with Flip	-
H	L	H	L	L	4-lane custom	-
H	L	H	L	H	4-lane custom with Flip	-
H	L	H	H	L	1-port USB 3.2 + 2-lane custom	-
H	L	H	H	H	1-port USB 3.2 + 2-lane custom with Flip	-
USB + Custom alternate mode (Sink side)						
H	H	L	L	L	Power Down	-
H	H	L	L	H	Power Down	-
H	H	L	H	L	1-port USB 3.2	-
H	H	L	H	H	1-port USB 3.2 with Flip	-
H	H	H	L	L	4-lane custom	-
H	H	H	L	H	4-lane custom with Flip	-
H	H	H	H	L	1-port USB 3.2 + 2-lane custom	-
H	H	H	H	H	1-port USB 3.2 + 2-lane custom with Flip	-

Table 22 GPIO configuration – AUXP/N-to-SBU1/2 mapping

CTL1	FLIP	Mapping
H	L	AUXP to SBU1, AUXN to SBU2
	H	AUXP to SBU2, AUXN to SBU1
L	X	Open

Table 23 Mux routing (Valid in GPIO mode or in I2C mode with CH_SWAP_SEL = 4'b0000 or 4'b1111)

DIR1	DIR0	CTL1	CTL0	FLIP	SWAP = L			SWAP = H		
					EQ	Input	Output	EQ	Input	Output
USB + DP alternate mode (Source side)										
L	L	L	L	L	NA	NA	NA	NA	NA	NA
L	L	L	L	H	NA	NA	NA	NA	NA	NA
L	L	L	H	L	DEQ[1:0]	DRX1P	URX1P (SSRXP)	DEQ[1:0]	URX1P (SSTXP)	DRX1P
					DEQ[1:0]	DRX1N	URX1N (SSRXN)	DEQ[1:0]	URX1N (SSTXN)	DRX1N
					UEQ[1:0]	UTX1P (SSTXP)	DTX1P	UEQ[1:0]	DTX1P	UTX1P (SSRXP)
					UEQ[1:0]	UTX1N (SSTXN)	DTX1N	UEQ[1:0]	DTX1N	UTX1N (SSRXN)
L	L	L	H	H	DEQ[1:0]	DRX2P	URX2P (SSRXP)	DEQ[1:0]	URX2P (SSTXP)	DRX2P
					DEQ[1:0]	DRX2N	URX2N (SSRXN)	DEQ[1:0]	URX2N (SSTXN)	DRX2N
					UEQ[1:0]	UTX2P (SSTXP)	DTX2P	UEQ[1:0]	DTX2P	UTX2P (SSRXP)
					UEQ[1:0]	UTX2N (SSTXN)	DTX2N	UEQ[1:0]	DTX2N	UTX2N (SSRXN)
L	L	H	L	L	UEQ[1:0]	URX2P (DP0P)	DRX2P	UEQ[1:0]	DRX2P	URX2P (DP0P)
					UEQ[1:0]	URX2N (DP0N)	DRX2N	UEQ[1:0]	DRX2N	URX2N (DP0N)
					UEQ[1:0]	UTX2P (DP1P)	DTX2P	UEQ[1:0]	DTX2P	UTX2P (DP1P)
					UEQ[1:0]	UTX2N (DP1N)	DTX2N	UEQ[1:0]	DTX2N	UTX2N (DP1N)
					UEQ[1:0]	UTX1P (DP2P)	DTX1P	UEQ[1:0]	DTX1P	UTX1P (DP2P)
					UEQ[1:0]	UTX1N (DP2N)	DTX1N	UEQ[1:0]	DTX1N	UTX1N (DP2N)
					UEQ[1:0]	URX1P (DP3P)	DRX1P	UEQ[1:0]	DRX1P	URX1P (DP3P)
					UEQ[1:0]	URX1N (DP3N)	DRX1N	UEQ[1:0]	DRX1N	URX1N (DP3N)
L	L	H	L	H	UEQ[1:0]	URX1P (DP0P)	DRX1P	UEQ[1:0]	DRX1P	URX1P (DP0P)
					UEQ[1:0]	URX1N (DP0N)	DRX1N	UEQ[1:0]	DRX1N	URX1N (DP0N)
					UEQ[1:0]	UTX1P (DP1P)	DTX1P	UEQ[1:0]	DTX1P	UTX1P (DP1P)

DIR1	DIR0	CTL1	CTL0	FLIP	SWAP = L			SWAP = H		
					EQ	Input	Output	EQ	Input	Output
					UEQ[1:0]	UTX1N (DP1N)	DTX1N	UEQ[1:0]	DTX1N	UTX1N (DP1N)
					UEQ[1:0]	UTX2P (DP2P)	DTX2P	UEQ[1:0]	DTX2P	UTX2P (DP2P)
					UEQ[1:0]	UTX2N (DP2N)	DTX2N	UEQ[1:0]	DTX2N	UTX2N (DP2N)
					UEQ[1:0]	URX2P (DP3P)	DRX2P	UEQ[1:0]	DRX2P	URX2P (DP3P)
					UEQ[1:0]	URX2N (DP3N)	DRX2N	UEQ[1:0]	DRX2N	URX2N (DP3N)
L	L	H	H	L	DEQ[1:0]	DRX1P	URX1P (SSRXP)	DEQ[1:0]	URX1P (SSTXP)	DRX1P
					DEQ[1:0]	DRX1N	URX1N (SSRXN)	DEQ[1:0]	URX1N (SSTXN)	DRX1N
					UEQ[1:0]	UTX1P (SSTXP)	DTX1P	UEQ[1:0]	DTX1P	UTX1P (SSRXP)
					UEQ[1:0]	UTX1N (SSTXN)	DTX1N	UEQ[1:0]	DTX1N	UTX1N (SSRXN)
					UEQ[1:0]	URX2P (DP0P)	DRX2P	UEQ[1:0]	DRX2P	URX2P (DP0P)
					UEQ[1:0]	URX2N (DP0N)	DRX2N	UEQ[1:0]	DRX2N	URX2N (DP0N)
					UEQ[1:0]	UTX2P (DP1P)	DTX2P	UEQ[1:0]	DTX2P	UTX2P (DP1P)
					UEQ[1:0]	UTX2N (DP1N)	DTX2N	UEQ[1:0]	DTX2N	UTX2N (DP1N)
L	L	H	H	H	DEQ[1:0]	DRX2P	URX2P (SSRXP)	DEQ[1:0]	URX2P (SSTXP)	DRX2P
					DEQ[1:0]	DRX2N	URX2N (SSRXN)	DEQ[1:0]	URX2N (SSTXN)	DRX2N
					UEQ[1:0]	UTX2P (SSTXP)	DTX2P	UEQ[1:0]	DTX2P	UTX2P (SSRXP)
					UEQ[1:0]	UTX2N (SSTXN)	DTX2N	UEQ[1:0]	DTX2N	UTX2N (SSRXN)
					UEQ[1:0]	URX1P (DP0P)	DRX1P	UEQ[1:0]	DRX1P	URX1P (DP0P)
					UEQ[1:0]	URX1N (DP0N)	DRX1N	UEQ[1:0]	DRX1N	URX1N (DP0N)
					UEQ[1:0]	UTX1P (DP1P)	DTX1P	UEQ[1:0]	DTX1P	UTX1P (DP1P)
					UEQ[1:0]	UTX1N (DP1N)	DTX1N	UEQ[1:0]	DTX1N	UTX1N (DP1N)
USB + DP alternate mode (Sink side)										
L	L	L	L	L	NA	NA	NA	NA	NA	NA
L	L	L	L	H	NA	NA	NA	NA	NA	NA
L	L	L	H	L	UEQ[1:0]	UTX2P	DTX2P (SSRXP)	UEQ[1:0]	DTX2P (SSTXP)	UTX2P

DIR1	DIR0	CTL1	CTL0	FLIP	SWAP = L			SWAP = H		
					EQ	Input	Output	EQ	Input	Output
					UEQ[1:0]	UTX2N	DTX2N (SSRXN)	UEQ[1:0]	DTX2N (SSTXN)	UTX2N
					DEQ[1:0]	DRX2P (SSTXP)	URX2P	DEQ[1:0]	URX2P	DRX2P (SSRXP)
					DEQ[1:0]	DRX2N (SSTXN)	URX2N	DEQ[1:0]	URX2N	DRX2N (SSRXN)
L	L	L	H	H	UEQ[1:0]	UTX1P	DTX1P (SSRXP)	UEQ[1:0]	DTX1P (SSTXP)	UTX1P
					UEQ[1:0]	UTX1N	DTX1N (SSRXN)	UEQ[1:0]	DTX1N (SSTXN)	UTX1N
					DEQ[1:0]	DRX1P (SSTXP)	URX1P	DEQ[1:0]	URX1P	DRX1P (SSRXP)
					DEQ[1:0]	DRX1N (SSTXN)	URX1N	DEQ[1:0]	URX1N	DRX1N (SSRXN)
L	L	H	L	L	UEQ[1:0]	URX2P	DRX2P (DP3P)	UEQ[1:0]	DRX2P (DP3P)	URX2P
					UEQ[1:0]	URX2N	DRX2N (DP3N)	UEQ[1:0]	DRX2N (DP3N)	URX2N
					UEQ[1:0]	UTX2P	DTX2P (DP2P)	UEQ[1:0]	DTX2P (DP2P)	UTX2P
					UEQ[1:0]	UTX2N	DTX2N (DP2N)	UEQ[1:0]	DTX2N (DP2N)	UTX2N
					UEQ[1:0]	UTX1P	DTX1P (DP1P)	UEQ[1:0]	DTX1P (DP1P)	UTX1P
					UEQ[1:0]	UTX1N	DTX1N (DP1N)	UEQ[1:0]	DTX1N (DP1N)	UTX1N
					UEQ[1:0]	URX1P	DRX1P (DP0P)	UEQ[1:0]	DRX1P (DP0P)	URX1P
					UEQ[1:0]	URX1P	DRX1N (DP0P)	UEQ[1:0]	DRX1N (DP0N)	URX1N
L	L	H	L	H	UEQ[1:0]	URX1P	DRX1P (DP3P)	UEQ[1:0]	DRX1P (DP3P)	URX1P
					UEQ[1:0]	URX1N	DRX1N (DP3N)	UEQ[1:0]	DRX1N (DP3N)	URX1N
					UEQ[1:0]	UTX1P	DTX1P (DP2P)	UEQ[1:0]	DTX1P (DP2P)	UTX1P
					UEQ[1:0]	UTX1N	DTX1N (DP2N)	UEQ[1:0]	DTX1N (DP2N)	UTX1N
					UEQ[1:0]	UTX2P	DTX2P (DP1P)	UEQ[1:0]	DTX2P (DP1P)	UTX2P
					UEQ[1:0]	UTX2N	DTX2N (DP1N)	UEQ[1:0]	DTX2N (DP1N)	UTX2N
					UEQ[1:0]	URX2P	DRX2P (DP0P)	UEQ[1:0]	DRX2P (DP0P)	URX2P
					UEQ[1:0]	URX2N	DRX2N (DP0N)	UEQ[1:0]	DRX2N (DP0N)	URX2N
L	L	H	H	L	DEQ[1:0]	DRX2P (SSRXP)	URX2P	DEQ[1:0]	URX2P	DRX2P (SSRXP)

DIR1	DIR0	CTL1	CTL0	FLIP	SWAP = L			SWAP = H		
					EQ	Input	Output	EQ	Input	Output
					DEQ[1:0]	DRX2N (SSRXN)	URX2N	DEQ[1:0]	URX2N	DRX2N (SSRXN)
					UEQ[1:0]	UTX2P	DTX2P (SSTXP)	UEQ[1:0]	DTX2P (SSTXP)	UTX2P
					UEQ[1:0]	UTX2N	DTX2N (SSTXN)	UEQ[1:0]	DTX2N (SSTXN)	UTX2N
					UEQ[1:0]	URX1P	DRX1P (DP0P)	UEQ[1:0]	DRX1P (DP0P)	URX1P
					UEQ[1:0]	URX1N	DRX1N (DP0N)	UEQ[1:0]	DRX1N (DP0N)	URX1N
					UEQ[1:0]	UTX1P	DTX1P (DP1P)	UEQ[1:0]	DTX1P (DP1P)	UTX1P
					UEQ[1:0]	UTX1N	DTX1N (DP1N)	UEQ[1:0]	DTX1N (DP1N)	UTX1N
L	L	H	H	H	DEQ[1:0]	DRX1P (SSRXP)	URX1P	DEQ[1:0]	URX1P	DRX1P (SSRXP)
					DEQ[1:0]	DRX1N (SSRXN)	URX1N	DEQ[1:0]	URX1N	DRX1N (SSRXN)
					UEQ[1:0]	UTX1P	DTX1P (SSTXP)	UEQ[1:0]	DTX1P (SSTXP)	UTX1P
					UEQ[1:0]	UTX1N	DTX1N (SSTXN)	UEQ[1:0]	DTX1N (SSTXN)	UTX1N
					UEQ[1:0]	URX2P	DRX2P (DP0P)	UEQ[1:0]	DRX2P (DP0P)	URX2P
					UEQ[1:0]	URX2N	DRX2N (DP0N)	UEQ[1:0]	DRX2N (DP0N)	URX2N
					UEQ[1:0]	UTX2P	DTX2P (DP1P)	UEQ[1:0]	DTX2P (DP1P)	UTX2P
					UEQ[1:0]	UTX2N	DTX2N (DP1N)	UEQ[1:0]	DTX2N (DP1N)	UTX2N
USB + Custom alternate mode (Source side)										
L	L	L	L	L	NA	NA	NA	NA	NA	NA
L	L	L	L	H	NA	NA	NA	NA	NA	NA
L	L	L	H	L	DEQ[1:0]	DRX1P	URX1P (SSRXP)	DEQ[1:0]	URX1P (SSTXP)	DRX1P
					DEQ[1:0]	DRX1N	URX1N (SSRXN)	DEQ[1:0]	URX1N (SSTXN)	DRX1N
					UEQ[1:0]	UTX1P (SSTXP)	DTX1P	UEQ[1:0]	DTX1P	UTX1P (SSRXP)
					UEQ[1:0]	UTX1N (SSTXN)	DTX1N	UEQ[1:0]	DTX1N	UTX1N (SSRXN)
L	L	L	H	H	DEQ[1:0]	DRX2P	URX2P (SSRXP)	DEQ[1:0]	URX2P (SSTXP)	DRX2P
					DEQ[1:0]	DRX2N	URX2N (SSRXN)	DEQ[1:0]	URX2N (SSTXN)	DRX2N
					UEQ[1:0]	UTX2P (SSTXP)	DTX2P	UEQ[1:0]	DTX2P	UTX2P (SSRXP)

DIR1	DIR0	CTL1	CTL0	FLIP	SWAP = L			SWAP = H		
					EQ	Input	Output	EQ	Input	Output
					UEQ[1:0]	UTX2N (SSTXN)	DTX2N	UEQ[1:0]	DTX2N	UTX2N (SSRXN)
L	L	H	L	L	DEQ[1:0]	DRX2P	URX2P (LN1RXP)	DEQ[1:0]	URX2P (LN1RXP)	DRX2P
					DEQ[1:0]	DRX2N	URX2N (LN1RXN)	DEQ[1:0]	URX2N (LN1RXN)	DRX2N
					UEQ[1:0]	UTX2P (LN1TXP)	DTX2P	UEQ[1:0]	DTX2P	UTX2P (LN1TXP)
					UEQ[1:0]	UTX2N (LN1TXN)	DTX2N	UEQ[1:0]	DTX2N	UTX2N (LN1TXN)
					UEQ[1:0]	UTX1P (LN0TXP)	DTX1P	UEQ[1:0]	DTX1P	UTX1P (LN0TXP)
					UEQ[1:0]	UTX1N (LN0TXN)	DTX1N	UEQ[1:0]	DTX1N	UTX1N (LN0TXN)
					DEQ[1:0]	DRX1P	URX1P (LN0RXP)	DEQ[1:0]	URX1P (LN0RXP)	DRX1P
					DEQ[1:0]	DRX1N	URX1N (LN0RXN)	DEQ[1:0]	URX1N (LN0RXN)	DRX1N
L	L	H	L	H	DEQ[1:0]	DRX1P	URX1P (LN1RXP)	DEQ[1:0]	URX1P (LN1RXP)	DRX1P
					DEQ[1:0]	DRX1N	URX1N (LN1RXN)	DEQ[1:0]	URX1N (LN1RXN)	DRX1N
					UEQ[1:0]	UTX1P (LN1TXP)	DTX1P	UEQ[1:0]	DTX1P	UTX1P (LN1TXP)
					UEQ[1:0]	UTX1N (LN1TXN)	DTX1N	UEQ[1:0]	DTX1N	UTX1N (LN1TXN)
					UEQ[1:0]	UTX2P (LN0TXP)	DTX2P	UEQ[1:0]	DTX2P	UTX2P (LN0TXP)
					UEQ[1:0]	UTX2N (LN0TXN)	DTX2N	UEQ[1:0]	DTX2N	UTX2N (LN0TXN)
					DEQ[1:0]	DRX2P	URX2P (LN0RXP)	DEQ[1:0]	URX2P (LN0RXP)	DRX2P
					DEQ[1:0]	DRX2N	URX2N (LN0RXN)	DEQ[1:0]	URX2N (LN0RXN)	DRX2N
L	L	H	H	L	DEQ[1:0]	DRX1P	URX1P (SSRXP)	DEQ[1:0]	URX1P (SSTXP)	DRX1P
					DEQ[1:0]	DRX1N	URX1N (SSRXN)	DEQ[1:0]	URX1N (SSTXN)	DRX1N
					UEQ[1:0]	UTX1P (SSTXP)	DTX1P	UEQ[1:0]	DTX1P	UTX1P (SSRXP)
					UEQ[1:0]	UTX1N (SSTXN)	DTX1N	UEQ[1:0]	DTX1N	UTX1N (SSRXN)
					UEQ[1:0]	UTX2P (LN0TXP)	DTX2P	UEQ[1:0]	DTX2P	UTX2P (LN0TXP)
					UEQ[1:0]	UTX2N (LN0TXN)	DTX2N	UEQ[1:0]	DTX2N	UTX2N (LN0TXN)
					DEQ[1:0]	DRX2P	URX2P (LN0RXP)	DEQ[1:0]	URX2P (LN0RXP)	DRX2P

DIR1	DIR0	CTL1	CTL0	FLIP	SWAP = L			SWAP = H		
					EQ	Input	Output	EQ	Input	Output
					DEQ[1:0]	DRX2N	URX2N (LN0RXN)	DEQ[1:0]	URX2N (LN0RXN)	DRX2N
L	L	H	H	H	DEQ[1:0]	DRX2P	URX2P (SSRXP)	DEQ[1:0]	URX2P (SSTXP)	DRX2P
					DEQ[1:0]	DRX2N	URX2N (SSRXN)	DEQ[1:0]	URX2N (SSTXN)	DRX2N
					UEQ[1:0]	UTX2P (SSTXP)	DTX2P	UEQ[1:0]	DTX2P	UTX2P (SSRXP)
					UEQ[1:0]	UTX2N (SSTXN)	DTX2N	UEQ[1:0]	DTX2N	UTX2N (SSRXN)
					UEQ[1:0]	UTX1P (LN0TXP)	DTX1P	UEQ[1:0]	DTX1P	UTX1P (LN0TXP)
					UEQ[1:0]	UTX1N (LN0TXN)	DTX1N	UEQ[1:0]	DTX1N	UTX1N (LN0TXN)
					DEQ[1:0]	DRX1P	URX1P (LN0RXP)	DEQ[1:0]	URX1P (LN0RXP)	DRX1P
					DEQ[1:0]	DRX1N	URX1N (LN0RXN)	DEQ[1:0]	URX1N (LN0RXN)	DRX1N
USB + Custom alternate mode (Sink side)										
L	L	L	L	L	NA	NA	NA	NA	NA	NA
L	L	L	L	H	NA	NA	NA	NA	NA	NA
L	L	L	H	L	UEQ[1:0]	UTX2P	DTX2P (SSRXP)	UEQ[1:0]	DTX2P (SSTXP)	UTX2P
					UEQ[1:0]	UTX2N	DTX2N (SSRXN)	UEQ[1:0]	DTX2N (SSTXN)	UTX2N
					DEQ[1:0]	DRX2P (SSTXP)	URX2P	DEQ[1:0]	URX2P	DRX2P (SSRXP)
					DEQ[1:0]	DRX2N (SSTXN)	URX2N	DEQ[1:0]	URX2N	DRX2N (SSRXN)
L	L	L	H	H	UEQ[1:0]	UTX1P	DTX1P (SSRXP)	UEQ[1:0]	DTX1P (SSTXP)	UTX1P
					UEQ[1:0]	UTX1N	DTX1N (SSRXN)	UEQ[1:0]	DTX1N (SSTXN)	UTX1N
					DEQ[1:0]	DRX1P (SSTXP)	URX1P	DEQ[1:0]	URX1P	DRX1P (SSRXP)
					DEQ[1:0]	DRX1N (SSTXN)	URX1N	DEQ[1:0]	URX1N	DRX1N (SSRXN)
L	L	H	L	L	DEQ[1:0]	DRX2P	URX2P (LN1TXP)	DEQ[1:0]	URX2P (LN1TXP)	DRX2P
					DEQ[1:0]	DRX2N	URX2N (LN1TXN)	DEQ[1:0]	URX2N (LN1TXN)	DRX2N
					UEQ[1:0]	UTX2P (LN1RXP)	DTX2P	UEQ[1:0]	DTX2P	UTX2P (LN1RXP)
					UEQ[1:0]	UTX2N (LN1RXN)	DTX2N	UEQ[1:0]	DTX2N	UTX2N (LN1RXN)
					UEQ[1:0]	UTX1P (LN0RXP)	DTX1P	UEQ[1:0]	DTX1P	UTX1P (LN0RXP)

DIR1	DIR0	CTL1	CTL0	FLIP	SWAP = L			SWAP = H		
					EQ	Input	Output	EQ	Input	Output
					UEQ[1:0]	UTX1N (LN0RXN)	DTX1N	UEQ[1:0]	DTX1N	UTX1N (LN0RXN)
					DEQ[1:0]	DRX1P	URX1P (LN0RXP)	DEQ[1:0]	URX1P (LN0RXP)	DRX1P
					DEQ[1:0]	DRX1N	URX1N (LN0RXN)	DEQ[1:0]	URX1N (LN0RXN)	DRX1N
L	L	H	L	H	DEQ[1:0]	DRX2P	URX2P (LN0RXP)	DEQ[1:0]	URX2P (LN0RXP)	DRX2P
					DEQ[1:0]	DRX2N	URX2N (LN0RXN)	DEQ[1:0]	URX2N (LN0RXN)	DRX2N
					UEQ[1:0]	UTX2P (LN0RXP)	DTX2P	UEQ[1:0]	DTX2P	UTX2P (LN0RXP)
					UEQ[1:0]	UTX2N (LN0RXN)	DTX2N	UEQ[1:0]	DTX2N	UTX2N (LN0RXN)
					UEQ[1:0]	UTX1P (LN0RXP)	DTX1P	UEQ[1:0]	DTX1P	UTX1P (LN0RXP)
					UEQ[1:0]	UTX1N (LN0RXN)	DTX1N	UEQ[1:0]	DTX1N	UTX1N (LN0RXN)
					DEQ[1:0]	DRX1P	URX1P (LN0TXP)	DEQ[1:0]	URX1P (LN0TXP)	DRX1P
					DEQ[1:0]	DRX1N	URX1N (LN0TXN)	DEQ[1:0]	URX1N (LN0TXN)	DRX1N
L	L	H	H	L	UEQ[1:0]	UTX2P	DTX2P (SSRXP)	UEQ[1:0]	DTX2P (SSTXP)	UTX2P
					UEQ[1:0]	UTX2N	DTX2N (SSRXN)	UEQ[1:0]	DTX2N (SSTXN)	UTX2N
					DEQ[1:0]	DRX2P (SSTXP)	URX2P	DEQ[1:0]	URX2P	DRX2P (SSRXP)
					DEQ[1:0]	DRX2N (SSTXN)	URX2N	DEQ[1:0]	URX2N	DRX2N (SSRXN)
					UEQ[1:0]	UTX1P	DTX1P (LN0RXP)	UEQ[1:0]	DTX1P (LN0RXP)	UTX1P
					UEQ[1:0]	UTX1N	DTX1N(L N0R XN)	UEQ[1:0]	DTX1N(LN 0R XN)	UTX1N
					DEQ[1:0]	DRX1P (LN0TXP)	URX1P	DEQ[1:0]	URX1P	DRX1P (LN0TXP)
					DEQ[1:0]	DRX1N (LN0TXN)	URX1N	DEQ[1:0]	URX1N	DRX1N (LN0TXN)
L	L	H	H	H	UEQ[1:0]	UTX1P	DTX1P (SSRXP)	UEQ[1:0]	DTX1P (SSSXP)	UTX1P
					UEQ[1:0]	UTX1N	DTX1N (SSRXN)	UEQ[1:0]	DTX1N (SSSXN)	UTX1N
					DEQ[1:0]	DRX1P (SSTXP)	URX1P	DEQ[1:0]	URX1P	DRX1P (SSRXP)
					DEQ[1:0]	DRX1N (SSTXN)	URX1N	DEQ[1:0]	URX1N	DRX1N (SSRXN)
					DEQ[1:0]	DRX2P	URX2P (LN0TXP)	DEQ[1:0]	URX2P (LN0TXP)	DRX2P

DIR1	DIR0	CTL1	CTL0	FLIP	SWAP = L			SWAP = H		
					EQ	Input	Output	EQ	Input	Output
					DEQ[1:0]	DRX2N	URX2N (LN0TXN)	DEQ[1:0]	URX2N (LN0TXN)	DRX2N
					UEQ[1:0]	UTX2P (LN0RXP)	DTX2P	UEQ[1:0]	DTX2P	UTX2P (LN0RXP)
					UEQ[1:0]	UTX2N (LN0RXN)	DTX2N	UEQ[1:0]	DTX2N	UTX2N (LN0RXN)

8.3.4 Device Configuration in I2C Mode

The configurations in I2C mode (I2CEN = 1) are all the same as the ones in GPIO mode. Refer to **Table 24** for the configuration of USB 3.2, Display Port and Custom Alternate Mode. Refer to **Table 25** to set the mapping between AUXP/N and SBU1/2.

Table 24 I2C configuration – device mode control

Register DIRSEL[1:0]	Register CTLSEL[1:0]	Register FLIPSEL	Device Configuration	VESA DP Alt Mode DFP_D Configuration
USB + DP Alternate Mode (Source side)				
00	00	0	Power Down	-
00	00	1	Power Down	-
00	01	0	1-port USB 3.2	-
00	01	1	1-port USB 3.2 with Flip	-
00	10	0	4-lane DP	C and E
00	10	1	4-lane DP with Flip	C and E
00	11	0	1-port USB 3.2 + 2-lane DP	D and F
00	11	1	1-port USB 3.2 + 2-lane DP with Flip	D and F
USB + DP Alternate Mode (Sink side)				
01	00	0	Power Down	-
01	00	1	Power Down	-
01	01	0	1-port USB 3.2	-
01	01	1	1-port USB 3.2 with Flip	-
01	10	0	4-lane DP	C and E
01	10	1	4-lane DP with Flip	C and E
01	11	0	1-port USB 3.2 + 2-lane DP	D and F
01	11	1	1-port USB 3.2 + 2-lane DP with Flip	D and F
USB + Custom Alternate Mode (Source side)				
10	00	0	Power Down	-
10	00	1	Power Down	-
10	01	0	1-port USB 3.2	-
10	01	1	1-port USB 3.2 with Flip	-
10	10	0	4-lane custom	-
10	10	1	4-lane custom with Flip	-
10	11	0	1-port USB 3.2 + 2-lane custom	-
10	11	1	1-port USB 3.2 + 2-lane custom with Flip	-

Register DIRSEL[1:0]	Register CTLSEL[1:0]	Register FLIPSEL	Device Configuration	VESA DP Alt Mode DFP_D Configuration
USB + Custom Alternate Mode (Sink side)				
11	00	0	Power Down	-
11	00	1	Power Down	-
11	01	0	1-port USB 3.2	-
11	01	1	1-port USB 3.2 with Flip	-
11	10	0	4-lane custom	-
11	10	1	4-lane custom with Flip	-
11	11	0	1-port USB 3.2 + 2-lane custom	-
11	11	1	1-port USB 3.2 + 2-lane custom with Flip	-

Table 25 I2C configuration – AUXP/N-to-SBU1/2 mapping

Register AUX_SBU_OVR[1:0]	Register CTLSEL[1]	Register FLIPSEL	Mapping
00	0	-	Open
	1	0	AUXP to SBU1, AUXN to SBU2
		1	AUXP to SBU2, AUXN to SBU1
01	-	-	AUXP to SBU1, AUXN to SBU2
10	-	-	AUXP to SBU2, AUXN to SBU1
11	-	-	Open

Table 26 SCHQ674401A-QF4060 Receiver Equalization GPIO Control

	Downstream Facing Ports with 1.1V linearity setting				Upstream Facing Port with 1.1V linearity setting			
EQ stage	DEQ1 Setting	DEQ0 Setting	EQ Gain @ 5GHz / dB	EQ Gain @ 4.05GHz / dB	UEQ1 Setting	UEQ0 Setting	EQ Gain @ 5GHz / dB	EQ Gain @ 4.05GHz / dB
0	0	0	3.9	3.5	0	0	3.9	3.5
1	0	R	5.0	4.5	0	R	5.0	4.5
2	0	F	5.9	5.4	0	F	5.9	5.4
3	0	1	6.6	6.2	0	1	6.6	6.2
4	R	0	7.3	6.9	R	0	7.3	6.9
5	R	R	7.8	7.4	R	R	7.8	7.4
6	R	F	8.3	7.9	R	F	8.3	7.9
7	R	1	8.6	8.4	R	1	8.6	8.4
8	F	0	8.7	8.5	F	0	8.7	8.5
9	F	R	9.0	8.8	F	R	9.0	8.8
10	F	F	9.3	9.1	F	F	9.3	9.1
11	F	1	9.4	9.3	F	1	9.4	9.3
12	1	0	9.5	9.4	1	0	9.5	9.4
13	1	R	9.8	9.7	1	R	9.8	9.7
14	1	F	10.0	10.0	1	F	10.0	10.0
15	1	1	10.1	10.2	1	1	10.1	10.2

Table 27 DC Gain and VOD Linear Range

EQ stage	CFG1 Setting	CFG0 Setting	Downstream DC Gain / dB	Upstream DC Gain / dB	Downstream VOD Linear Range / V_{pp}	Upstream VOD Linear Range / V_{pp}
0	0	0	1	0	0.9	0.9
1	0	R	0	1	0.9	0.9
2	0	F	0	0	0.9	0.9
3	0	1	1	1	0.9	0.9
4	R	0	0	0	1.1	1.1
5	R	R	1	0	1.1	1.1
6	R	F	0	1	1.1	1.1
7	R	1	2	2	1.1	1.1
8	F	0	Rsvd.	Rsvd.	Rsvd.	Rsvd.
9	F	R	Rsvd.	Rsvd.	Rsvd.	Rsvd.
10	F	F	0	0	1.3	1.3
11	F	1	Rsvd.	Rsvd.	Rsvd.	Rsvd.
12	1	0	Rsvd.	Rsvd.	Rsvd.	Rsvd.
13	1	R	Rsvd.	Rsvd.	Rsvd.	Rsvd.
14	1	F	Rsvd.	Rsvd.	Rsvd.	Rsvd.
15	1	1	Rsvd.	Rsvd.	Rsvd.	Rsvd.

8.4 I2C Programming

Table 28 I2C Slave Address

UEQ1 Pin (A1)	UEQ0 Pin (A0)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (W/R)
0	0	1	0	0	0	1	0	0	0/1
0	R	1	0	0	0	1	0	1	0/1
0	F	1	0	0	0	1	1	0	0/1
0	1	1	0	0	0	1	1	1	0/1
R	0	0	1	0	0	0	0	0	0/1
R	R	0	1	0	0	0	0	1	0/1
R	F	0	1	0	0	0	1	0	0/1
R	1	0	1	0	0	0	1	1	0/1
F	0	0	0	1	0	0	0	0	0/1
F	R	0	0	1	0	0	0	1	0/1
F	F	0	0	1	0	0	1	0	0/1
F	1	0	0	1	0	0	1	1	0/1
1	0	0	0	0	1	1	0	0	0/1
1	R	0	0	0	1	1	0	1	0/1
1	F	0	0	0	1	1	1	0	0/1
1	1	0	0	0	1	1	1	1	0/1

8.4.1 How to write to SCHQ674401A I2C registers?

1) The I2C master initiates a write operation by sending a start condition (S), followed by transmitting the 7-bit address of the SCHQ674401A and a zero-value “W/R” bit to indicate a write cycle.
2) The SCHQ674401A acknowledges the address cycle.
3) Transmit the sub-address (register address within SCHQ674401A) to be written by the master, consisting of one byte of data, MSB-first.
4) The SCHQ674401A acknowledges the sub-address cycle.
5) Transmit the first byte of data to be written to the I2C register by the master.
6) The SCHQ674401A acknowledges the byte transfer.
7) The master may continue transmitting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the SCHQ674401A.
8) Terminate the write operation by the master generating a stop condition (P).

8.4.2 How to read from SCHQ674401A I2C registers with a sub-address of the register?

8.4.2.1 Setting the starting sub-address for I2C reads (Optional).

1) The I^{2}C master initiates a write operation by sending a start condition (S), followed by transmitting the 7-bit address of the SCHQ674401A and a zero-value “W/R” bit to indicate a write cycle.
2) The SCHQ674401A acknowledges the address cycle.
3) Transmit the sub-address (I2C register within SCHQ674401A) to be written by the master, consisting of one byte of data, MSB-first.
4) The SCHQ674401A acknowledges the sub-address cycle.
5) Terminate the write operation by the master generating a stop condition (P).

8.4.2.2 Reading the SCHQ674401A I2C registers.

1) The I2C master initiates a read operation by sending a start condition (S), followed by transmitting the 7-bit address of the SCHQ674401A and a one-value "W/R" bit to indicate a read cycle.
2) The SCHQ674401A acknowledges the address cycle.
3) If a write operation of setting the starting sub-address (following **8.4.2**) occurred prior to the read, then the SCHQ674401A starts at the sub-address specified in the write. Else, the SCHQ674401A transmits the contents of the memory registers in MSB-first order starting at register 00h or the last read sub-address+1.
4) After each byte transfer, the SCHQ674401A waits for either an acknowledgement (ACK) or a not-acknowledgement (NACK) from the master. The I2C master acknowledges reception of each data byte transfer.
5) If the SCHQ674401A receives an ACK, it transmits the next byte of data.
6) Terminate the write operation by the master generating a stop condition (P).

8.5 Register Maps

The memory-mapped registers for the SCHQ674401A are specified in **Table 29**. Any register offset address that is not listed in **Table 29** should be considered reserved, and the contents of the registers at these locations should not be modified.

Table 29 Register Maps

Offset	Acronym	Register Name	Section
0Ah	General-1	General Registers 1	Table 31
0Bh	General-2	General Registers 2	Table 32
0Ch	General-3	General Registers 3	Table 33
10h	UFP2-EQ	UFP2 EQ Control	Table 34
11h	UFP1-EQ	UFP1 EQ Control	Table 35
12h	DisplayPort-1	AUX Snoop Status	Table 36
13h	DisplayPort-2	DP Lane Enable/Disable Control	Table 37
1Bh	SOFT-RESET	I2C and DPCD Soft Resets	Table 38
20h	DFP2-EQ	DFP2 EQ Control	Table 39
21h	DFP1-EQ	DFP1 EQ Control	Table 40
22h	USB3	USB3 Control	Table 41
23h	USB3-LOS	USB3 LOS Threshold Control	Table 42

The access types that are used in this section are encoded into small table cells using bit codes. **Table 30** shows the codes that are utilized for the access types.

Table 30 SCHQ674401A-QF4060 Access Type Codes

Code	Description
R	Read
W	Write
H	Set or cleared by hardware
S	Self-clearing

Table 31 General-1 Register (Offset = 0Ah, Default = 1h)

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	00	Reserved
5	SWAP_SEL	R/W	0	Global direction swap for all channels. 0 = Channel directions and EQ settings are in normal mode, 1 = Reverse channel directions and EQ settings for input ports.
4	EQ_OVERRIDE	R/W	0	EQ setting source configuration. 0 = EQ settings from EQ pins, 1 = EQ settings from registers.
3	HPDIN_OVERRIDE	R/W	0	HPDIN pin state setting source configuration. 0 = HPD_IN based on HPD_IN pin, 1 = HPD_IN high.
2	FLIP_SEL	R/W	0	Orientation configuration. 0 = Normal orientation, 1 = Flip orientation.
1:0	CTLSEL[1:0]	R/W	01	DP and USB modes control. 00 = Disabled. All channels are disabled, 01 = USB3.1 only, 10 = 4-lane of DisplayPort, 11 = USB3.1 and 2-lane of DisplayPort.

Table 32 General-2 Register (Offset = 0Bh, reset = 0h)

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0000	Reserved
3:0	CH_SWAP_SEL	R/W	0000	Swaps direction (TX to Rx and Rx to Tx) and EQ settings of individual channels. Channels are numbered from 3 to 0. 1 bit per lane. 0 = Channel and EQ settings normal, 1 = Reverse channel direction and EQ setting.

Table 33 General-3 Register (Offset = 0Ch, reset = 0h)

Bit	Field	Type	Reset	Description
7	RESERVED	R	0	Reserved
6	VOD_DCGAIN_OVERRIDE	R/W	0	VOD linearity range and DC gain setting source configuration. 0 = VOD linearity and DC gain settings from CFG[2:1] pins 1 = VOD linearity and DC gain settings from registers
5:2	VOD_DCGAIN_SEL	R/W	0000	VOD linearity range and DC gain settings. When VOD_DCGAIN_OVERRIDE = 0b, this field reflects the sampled state of CFG[1:0] pins. 1b, these bits are configurable for CFG1 and CFG0. [5:4] = CFG1,[3:2] = CFG0. 00 = L, 01 = R, 10 = F, 11 = H.

Bit	Field	Type	Reset	Description
1:0	DIR_SEL	R/W	00	Operation mode. 00 = USB + DP Alt Mode Source, 01 = USB + DP Alt Mode Sink, 10 = USB + Custom Alt Mode Source, 11 = USB + Custom Alt Mode Sink.

Table 34 UFP2-EQ Register (Offset = 10h, reset = 0h)

Bit	Field	Type	Reset	Description
7:4	UTX2EQ_SEL	R/W	0000	EQ for UTX2P/N pins. When EQ_OVERRIDE = 0b, this field reflects the sampled state of UEQ[1:0] pins. 1b, these bits are configurable for EQ of UTX2P/N. [7:6] = UTX2_EQ1, [5:4] = UTX2_EQ0. 00 = L, 01 = R, 10 = F, 11 = H.
3:0	URX2EQ_SEL	R/W	0000	EQ for URX2P/N pins. When EQ_OVERRIDE = 0b, this field reflects the sampled state of UEQ[1:0] pins. 1b, these bits are configurable for EQ of URX2P/N. [3:2] = URX2_EQ1, [1:0] = URX2_EQ0. 00 = L, 01 = R, 10 = F, 11 = H.

Table 35 UFP1-EQ Register (Offset = 11h, reset = 0h)

Bit	Field	Type	Reset	Description
7:4	UTX1EQ_SEL	R/W	0000	EQ for UTX1P/N pins When EQ_OVERRIDE = 0b, this field reflects the sampled state of UEQ[1:0] pins. 1b, these bits are configurable for EQ of UTX1P/N. [7:6] = UTX1_EQ1, [5:4] = UTX1_EQ0. 00 = L, 01 = R, 10 = F, 11 = H.
3:0	URX1EQ_SEL	R/W	0000	EQ for URX1P/N pins When EQ_OVERRIDE = 0b, this field reflects the sampled state of UEQ[1:0] pins. 1b, these bits are configurable for EQ of URX1P/N. [3:2] = URX1_EQ1, [1:0] = URX1_EQ0. 00 = L, 01 = R, 10 = F, 11 = H.

Table 36 DisplayPort-1 Register (Offset = 12h, reset = 0h)

Bit	Field	Type	Reset	Description
7:5	SET_POWER_STATE	RH	000	Snooped value of the AUX writes to DPCD address 0x00600 When AUX_SNOOP_DISABLE = 0b, enable/disable state of DP lanes is based on the snooped value. 1b, DPx_DISABLE register (x = 0, 1, 2, or 3) controls the enable/disable state of each DP lane. This field is reset to 0h automatically when CTLSEL1 changes from 1b to 0b.
4:0	LANE_COUNT_SET	RH	00000	Snooped value of AUX writes to DPCD address 0x00101 When AUX_SNOOP_DISABLE = 0b, enable/disable state of DP lanes is based on the snooped value. Unused DP lanes will be disabled to save power. 1b, DPx_DISABLE register (x = 0, 1, 2, or 3) controls the enable/disable state of each DP lane. This field is reset to 0h automatically when CTLSEL1 changes from 1b to 0b.

Table 37 DisplayPort-2 Register (Offset = 13h, reset = 0h)

Bit	Field	Type	Reset	Description
7	AUX_SNOOP_DISABLE	R/W	0	DP lanes enabling source configuration 0 = AUX snooped value 1 = DP lanes are controlled by registers
6	RESERVED	R	0	Reserved
5:4	AUX_SBU_OVR	R/W	00	AUXP/N to SBU1/2 mapping setting source configuration 00 = AUX to SBU is determined by CTLSEL1 and FLIPSEL 01 = AUXP to SBU1 and AUXN to SBU2 10 = AUXP to SBU2 and AUXN to SBU1 11 = AUX to SBU open
3	DP3_DISABLE	R/W	0	DP lane 3 enable or disable configuration, only taking effect when AUX_SNOOP_DISABLE = 1b. 0 = DP Lane 3 enabled 1 = DP Lane 3 disabled
2	DP2_DISABLE	R/W	0	DP lane 2 enable or disable configuration, only taking effect when AUX_SNOOP_DISABLE = 1b. 0 = DP Lane 2 enabled 1 = DP Lane 2 disabled
1	DP1_DISABLE	R/W	0	DP lane 1 enable or disable configuration, only taking effect when AUX_SNOOP_DISABLE = 1b. 0 = DP Lane 1 enabled 1 = DP Lane 1 disabled
0	DP0_DISABLE	R/W	0	DP lane 0 enable or disable configuration, only taking effect when AUX_SNOOP_DISABLE = 1b. 0 = DP Lane 0 enabled 1 = DP Lane 0 disabled

Table 38 SOFT-RESET Register (Offset = 1Bh, reset = 0h)

Bit	Field	Type	Reset	Description
7	I2C_RST	RH/WS	0	Resets I2C registers to default values.
6	DPCD_RST	RH/WS	0	Resets DPCD registers to default values.
5:0	RESERVED	R	000000	Reserved

Table 39 DFP2-EQ Register (Offset = 20h, reset = 0h)

Bit	Field	Type	Reset	Description
7:4	DTX2EQ_SEL	R/W	0000	EQ for DTX2P/N pins When EQ_OVERRIDE = 0b, this field reflects the sampled state of DEQ[1:0] pins. 1b, these bits are configurable for EQ of DTX2P/N. [7:6] = DTX2_EQ1, [5:4] = DTX2_EQ0. 00 = L, 01 = R, 10 = F, 11 = H.
3:0	DRX2EQ_SEL	R/W	0000	EQ for DRX2P/N pins When EQ_OVERRIDE = 0b, this field reflects the sampled state of DEQ[1:0] pins. 1b, these bits are configurable for EQ of DRX2P/N. [3:2] = DRX2_EQ1, [1:0] = DRX2_EQ0, 00 = L, 01 = R, 10 = F, 11 = H.

Table 40 DFP1-EQ Register (Offset = 21h, reset = 0h)

Bit	Field	Type	Reset	Description
7:4	DTX1EQ_SEL	R/W	0000	EQ for DTX1P/N pins When EQ_OVERRIDE = 0b, this field reflects the sampled state of DEQ[1:0] pins. 1b, these bits are configurable for EQ of DTX1P/N. [7:6] = DTX1_EQ1, [5:4] = DTX1_EQ0. 00 = L, 01 = R, 10 = F, 11 = H.
3:0	DRX1EQ_SEL	R/W	0000	EQ for DRX1P/N pins When EQ_OVERRIDE = 0b, this field reflects the sampled state of DEQ[1:0] pins. 1b, these bits are configurable for EQ of DRX1P/N. [3:2] = DRX1_EQ1, [1:0] = DRX1_EQ0. 00 = L, 01 = R, 10 = F, 11 = H.

Table 41 USB3 Register (Offset = 22h, reset = 4h)

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	000	Reserved
4	DISABLE_U2U3_RXDET	R/W	0	Rx.Detect in U2/U3 state. 0 = Rx.Detect in U2/U3 enabled, 1 = Rx.Detect in U2/U3 disabled.
3:2	DFP_RXDET_INTERVAL	R/W	01	Rx.Detect interval for DFP (DTX1P/N and DTX2P/N) 00 = 3.62 ms, 01 = 5.4 ms, 10, 11 = Reserved
1:0	RESERVED	R	00	Reserved

Table 42 USB3-LOS Register (Offset = 23h, reset = 23h)

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	00000	Reserved
2:0	CFG_LOS_VTH	R/W	011	LOS assert threshold voltage 000 = 67 mV, 001 = 72 mV, 010 = 79 mV, 011 = 85 mV, 100 = 91 mV, 101 = 97 mV, 110 = 105 mV, 111 = 112 mV

9 Typical Application and Implementation

9.1 Typical Application Circuit

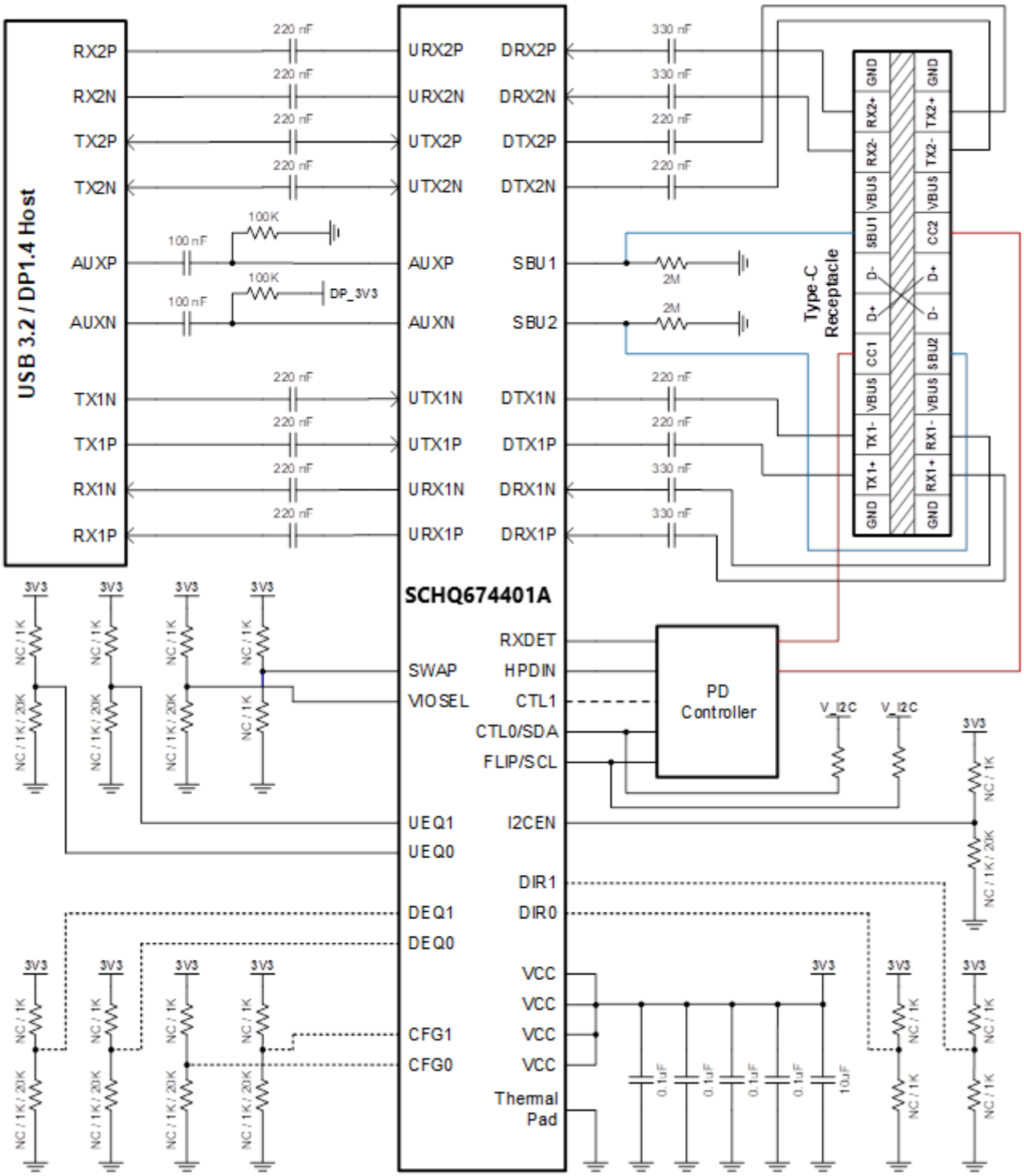


Figure 7 Typical Application Circuit

9.2 System Examples

9.2.1 USB/DP mode – 1-port USB 3.2 only

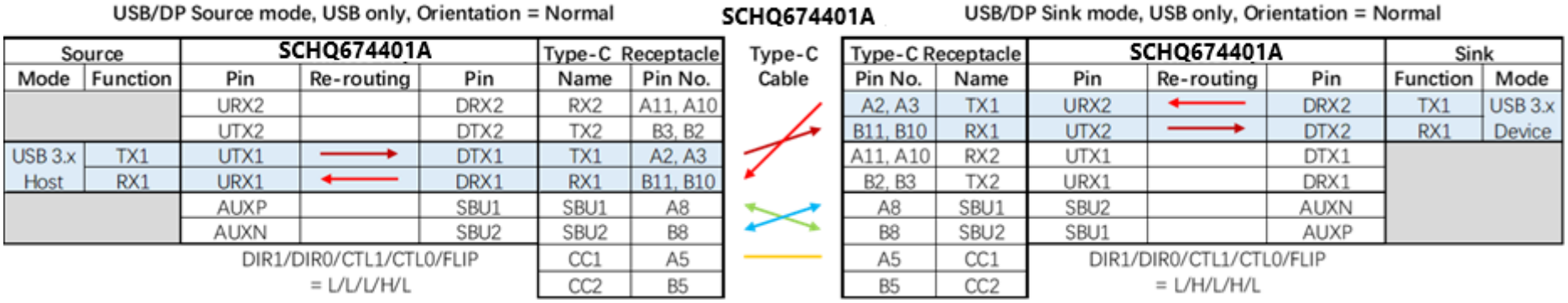


Figure 8 1-port USB 3.2 only (Orientation : Normal to Normal)

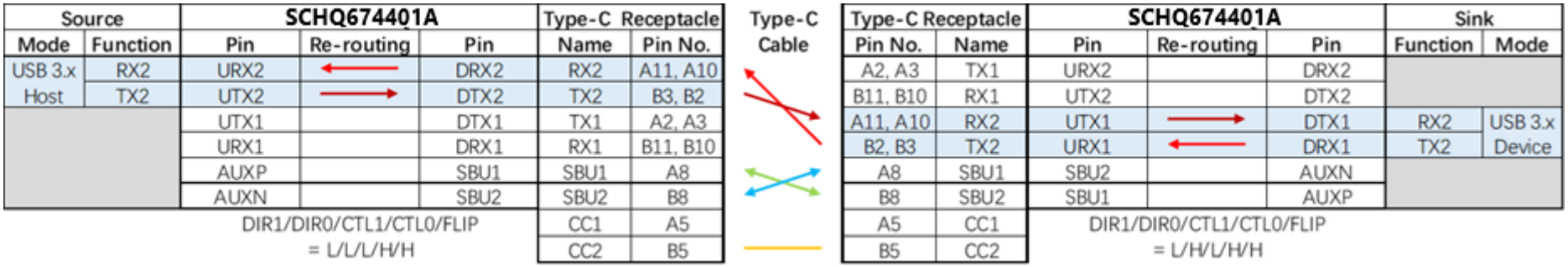


Figure 9 1-port USB 3.2 only (Orientation : Flip to Flip)

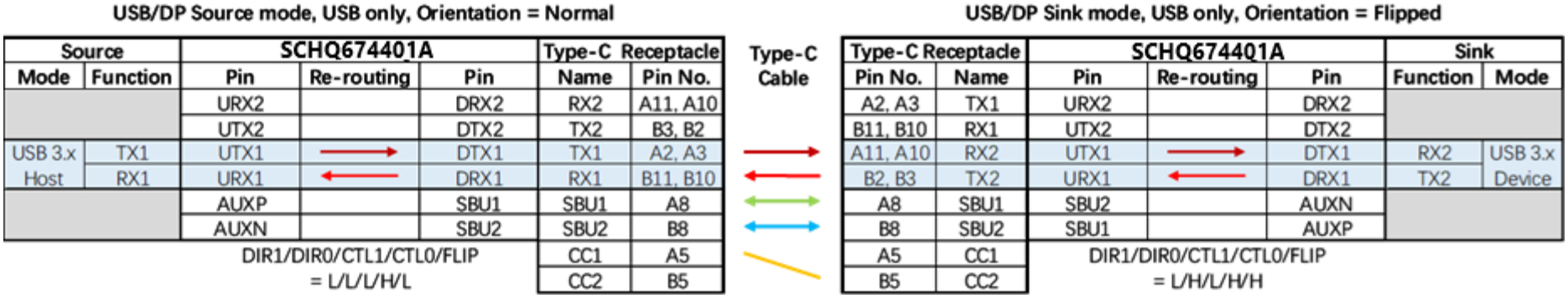


Figure 10 1-port USB 3.2 only (Orientation : Normal to Flip)

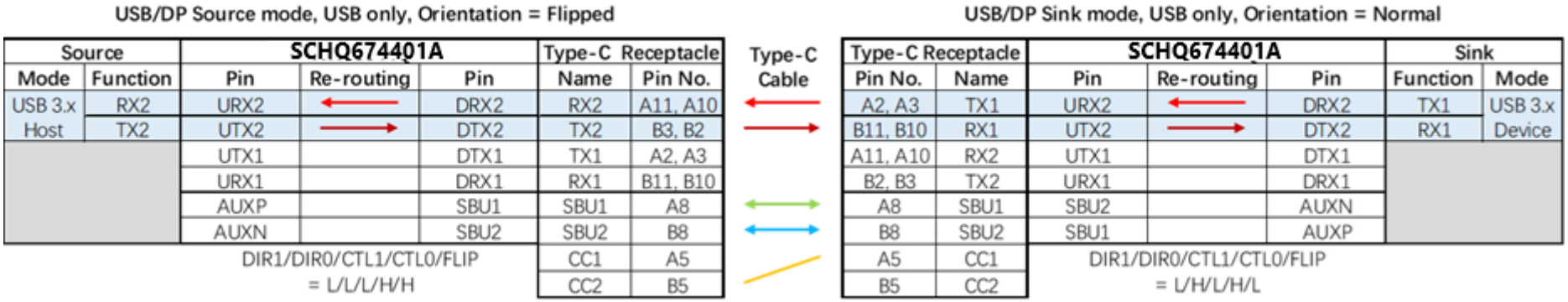


Figure 11 1-port USB 3.2 only (Orientation : Flip to Normal)

9.2.2 USB/DP mode – 1-port USB 3.2 + 2-lane DP

USB/DP Source mode, USB + 2-Lane DP, Orientation = Normal
(DFP_D Type-C Pin Assignment D)

Source		SCHQ674401A			Type-C Receptacle	
Mode	Function	Pin	Re-routing	Pin	Name	Pin No.
DP Source	ML0	URX2	→	DRX2	RX2	A11, A10
	ML1	UTX2	→	DTX2	TX2	B3, B2
USB 3.x Host	TX1	UTX1	→	DTX1	TX1	A2, A3
	RX1	URX1	←	DRX1	RX1	B11, B10
DP Source	AUXP	AUXP	→	SBU1	SBU1	A8
	AUXN	AUXN	←	SBU2	SBU2	B8
					CC1	A5
		DIR1/DIR0/CTL1/CTL0/FLIP = L/L/H/H/L			CC2	B5

Type-C Cable

USB/DP Sink mode, USB + 2-Lane DP, Orientation = Normal
(UFP_D Type-C Pin Assignment D)

Type-C Receptacle		SCHQ674401A			Sink	
Pin No.	Name	Pin	Re-routing	Pin	Function	Mode
A2, A3	TX1	URX2	←	DRX2	TX1	USB 3.x Device
B11, B10	RX1	UTX2	←	DTX2	RX1	
A11, A10	RX2	UTX1	→	DTX1	ML1	DP Sink
B2, B3	TX2	URX1	→	DRX1	ML0	
A8	SBU1	SBU2	←	AUXN	AUXN	
B8	SBU2	SBU1	→	AUXP	AUXP	
A5	CC1	DIR1/DIR0/CTL1/CTL0/FLIP = L/H/H/H/L				
B5	CC2					

Figure 12 1-port USB 3.2 + 2-lane DP (Orientation : Normal to Normal)

USB/DP Source mode, USB + 2-Lane DP, Orientation = Flipped
(DFP_D Type-C Pin Assignment D)

Source		SCHQ674401A			Type-C Receptacle	
Mode	Function	Pin	Re-routing	Pin	Name	Pin No.
USB 3.x Host	RX2	URX2	←	DRX2	RX2	A11, A10
	TX2	UTX2	→	DTX2	TX2	B3, B2
DP Source	ML1	UTX1	→	DTX1	TX1	A2, A3
	ML0	URX1	→	DRX1	RX1	B11, B10
	AUXP	AUXP	⇄	SBU1	SBU1	A8
	AUXN	AUXN	⇄	SBU2	SBU2	B8
					CC1	A5
		DIR1/DIR0/CTL1/CTL0/FLIP = L/L/H/H/H			CC2	B5

Type-C Cable

USB/DP Sink mode, USB + 2-Lane DP, Orientation = Flipped
(UFP_D Type-C Pin Assignment D)

Type-C Receptacle		SCHQ674401A			Sink	
Pin No.	Name	Pin	Re-routing	Pin	Function	Mode
A2, A3	TX1	URX2	→	DRX2	ML0	DP Sink
B11, B10	RX1	UTX2	→	DTX2	ML1	
A11, A10	RX2	UTX1	→	DTX1	RX2	USB 3.x Device
B2, B3	TX2	URX1	←	DRX1	TX2	
A8	SBU1	SBU2	⇄	AUXN	AUXN	DP Sink
B8	SBU2	SBU1	⇄	AUXP	AUXP	
A5	CC1	DIR1/DIR0/CTL1/CTL0/FLIP = L/H/H/H/H				
B5	CC2					

Figure 13 1-port USB 3.2 + 2-lane DP (Orientation : Flip to Flip)

USB/DP Source mode, USB + 2-Lane DP, Orientation = Normal
(DFP_D Type-C Pin Assignment D)

Source		SCHQ674401A			Type-C Receptacle	
Mode	Function	Pin	Re-routing	Pin	Name	Pin No.
DP Source	ML0	URX2	→	DRX2	RX2	A11, A10
	ML1	UTX2	→	DTX2	TX2	B3, B2
USB 3.x Host	TX1	UTX1	→	DTX1	TX1	A2, A3
	RX1	URX1	←	DRX1	RX1	B11, B10
DP Source	AUXP	AUXP	↔	SBU1	SBU1	A8
	AUXN	AUXN	↔	SBU2	SBU2	B8
		DIR1/DIR0/CTL1/CTL0/FLIP = L/L/H/H/L			CC1	A5
					CC2	B5

Type-C Cable

USB/DP Sink mode, USB + 2-Lane DP, Orientation = Flipped
(UFP_D Type-C Pin Assignment D)

Type-C Receptacle		SCHQ674401A			Sink	
Pin No.	Name	Pin	Re-routing	Pin	Function	Mode
A2, A3	TX1	URX2	→	DRX2	ML0	DP Sink
B11, B10	RX1	UTX2	→	DTX2	ML1	
A11, A10	RX2	UTX1	→	DTX1	RX2	USB 3.x Device
B2, B3	TX2	URX1	←	DRX1	TX2	
A8	SBU1	SBU2	↔	AUXN	AUXN	DP Sink
B8	SBU2	SBU1	↔	AUXP	AUXP	
A5	CC1	DIR1/DIR0/CTL1/CTL0/FLIP = L/H/H/H/H				
B5	CC2					

Figure 14 1-port USB 3.2 + 2-lane DP (Orientation : Normal to Flip)

USB/DP Source mode, USB + 2-Lane DP, Orientation = Flipped
(DFP_D Type-C Pin Assignment D)

Source		SCHQ674401A			Type-C Receptacle	
Mode	Function	Pin	Re-routing	Pin	Name	Pin No.
USB 3.x Host	RX2	URX2	←	DRX2	RX2	A11, A10
	TX2	UTX2	→	DTX2	TX2	B3, B2
DP Source	ML1	UTX1	→	DTX1	TX1	A2, A3
	ML0	URX1	→	DRX1	RX1	B11, B10
	AUXP	AUXP	↔	SBU1	SBU1	A8
	AUXN	AUXN	↔	SBU2	SBU2	B8
		DIR1/DIR0/CTL1/CTL0/FLIP = L/L/H/H/H			CC1	A5
					CC2	B5

Type-C Cable

USB/DP Sink mode, USB + 2-Lane DP, Orientation = Normal
(UFP_D Type-C Pin Assignment D)

Type-C Receptacle		SCHQ674401A			Sink	
Pin No.	Name	Pin	Re-routing	Pin	Function	Mode
A2, A3	TX1	URX2	←	DRX2	TX1	USB 3.x Device
B11, B10	RX1	UTX2	→	DTX2	RX1	
A11, A10	RX2	UTX1	→	DTX1	ML1	DP Sink
B2, B3	TX2	URX1	→	DRX1	ML0	
A8	SBU1	SBU2	↔	AUXN	AUXN	
B8	SBU2	SBU1	↔	AUXP	AUXP	
A5	CC1	DIR1/DIR0/CTL1/CTL0/FLIP = L/H/H/H/L				
B5	CC2					

Figure 15 1-port USB 3.2 + 2-lane DP (Orientation : Flip to Normal)

9.2.3 USB/DP mode – 4-lane DP

USB/DP Source mode, 4-Lane DP, Orientation = Normal
(DFP_D Type-C Pin Assignment C/E)

Source		SCHQ674401A			Type-C Receptacle	
Mode	Function	Pin	Re-routing	Pin	Name	Pin No.
DP Source	ML0	URX2	→	DRX2	RX2	A11, A10
	ML1	UTX2	→	DTX2	TX2	B2, B3
	ML2	UTX1	→	DTX1	TX1	A2, A3
	ML3	URX1	→	DRX1	RX1	B11, B10
	AUXP	AUXP	←	SBU1	SBU1	A8
	AUXN	AUXN	←	SBU2	SBU2	B8
	DIR1/DIR0/CTL1/CTL0/FLIP = L/L/H/L/L				CC1	A5
					CC2	B5

Type-C Cable

USB/DP Sink mode, 4-Lane DP, Orientation = Normal
(UFP_D Type-C Pin Assignment C)

Type-C Receptacle		SCHQ674401A			Sink	
Pin No.	Name	Pin	Re-routing	Pin	Function	Mode
A2, A3	TX1	URX2	→	DRX2	ML3	DP Sink
B11, B10	RX1	UTX2	→	DTX2	ML2	
A11, A10	RX2	UTX1	→	DTX1	ML1	
B2, B3	TX2	URX1	→	DRX1	ML0	
A8	SBU1	SBU2	←	AUXN	AUXN	
B8	SBU2	SBU1	←	AUXP	AUXP	
A5	CC1	DIR1/DIR0/CTL1/CTL0/FLIP = L/H/H/L/L				
B5	CC2					

Figure 16 4-lane DP (Orientation : Normal to Normal)

USB/DP Source mode, 4-Lane DP, Orientation = Flipped
(DFP_D Type-C Pin Assignment C/E)

Source		SCHQ674401A			Type-C Receptacle	
Mode	Function	Pin	Re-routing	Pin	Name	Pin No.
DP Source	ML3	URX2	→	DRX2	RX2	A11, A10
	ML2	UTX2	→	DTX2	TX2	B3, B2
	ML1	UTX1	→	DTX1	TX1	A2, A3
	ML0	URX1	→	DRX1	RX1	B11, B10
	AUXP	AUXP	⤫	SBU1	SBU1	A8
	AUXN	AUXN	⤫	SBU2	SBU2	B8
	DIR1/DIR0/CTL1/CTL0/FLIP = L/L/H/L/H				CC1	A5
					CC2	B5

Type-C Cable

USB/DP Sink mode, 4-Lane DP, Orientation = Flipped
(UFP_D Type-C Pin Assignment C)

Type-C Receptacle		SCHQ674401A			Sink	
Pin No.	Name	Pin	Re-routing	Pin	Function	Mode
A2, A3	TX1	URX2	→	DRX2	ML0	DP Sink
B11, B10	RX1	UTX2	→	DTX2	ML1	
A11, A10	RX2	UTX1	→	DTX1	ML2	
B2, B3	TX2	URX1	→	DRX1	ML3	
A8	SBU1	SBU2	⤫	AUXN	AUXN	
B8	SBU2	SBU1	⤫	AUXP	AUXP	
A5	CC1	DIR1/DIR0/CTL1/CTL0/FLIP = L/H/H/L/H				
B5	CC2					

Figure 17 4-lane DP (Orientation : Flip to Flip)

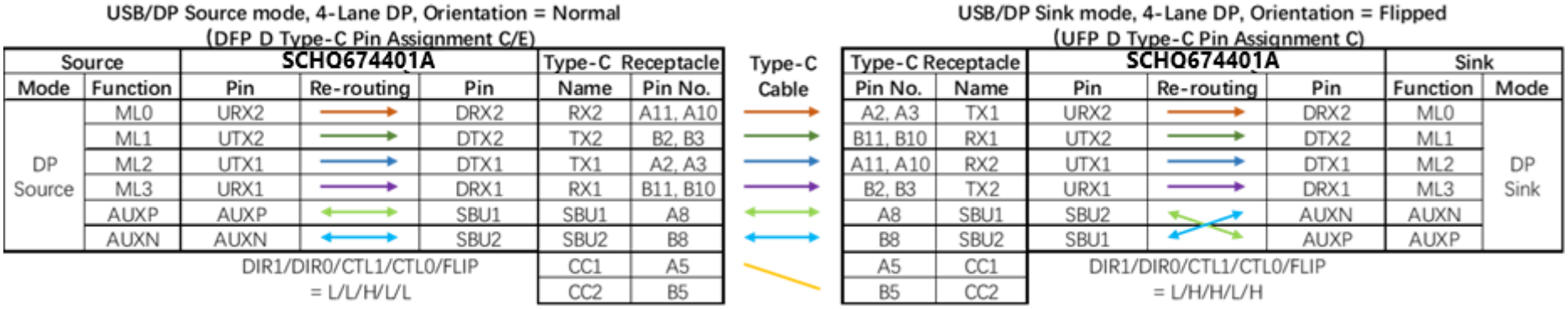


Figure 18 4-lane DP (Orientation : Normal to Flip)

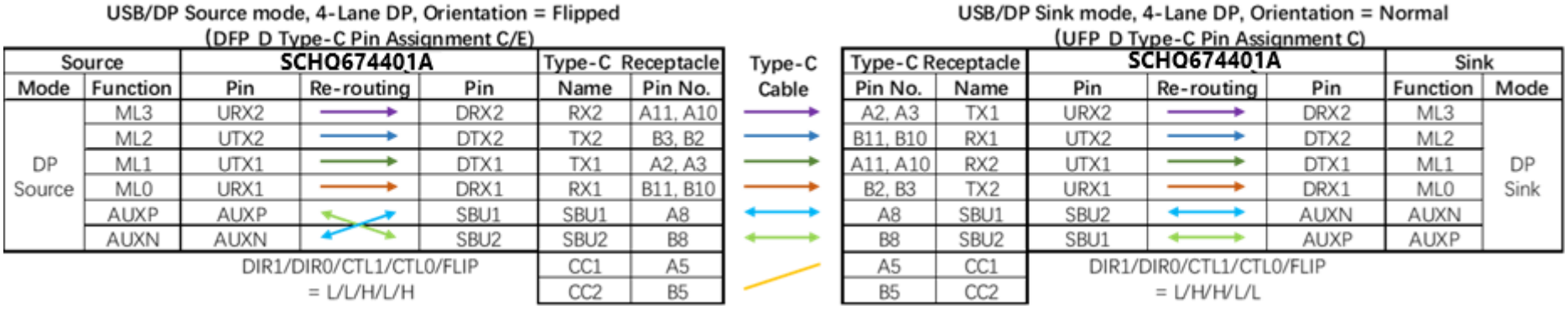


Figure 19 4-lane DP (Orientation : Flip to Normal)

9.2.4 USB/Custom mode – 1-port USB 3.2 + 2-lane Custom

USB/Custom Source mode, USB + 2-Lane Custom, Orientation = Normal

Source		SCHQ674401A			Type-C Receptacle	
Mode	Function	Pin	Re-routing	Pin	Name	Pin No.
Custom	LN0	URX2	←	DRX2	RX2	A11, A10
	LN1	UTX2	→	DTX2	TX2	B3, B2
USB 3.x Host	TX1	UTX1	→	DTX1	TX1	A2, A3
	RX1	URX1	←	DRX1	RX1	B11, B10
Custom	AUXP	AUXP	→	SBU1	SBU1	A8
	AUXN	AUXN	←	SBU2	SBU2	B8
DIR1/DIR0/CTL1/CTL0/FLIP = H/L/H/H/L					CC1	A5
					CC2	B5

Type-C Cable

USB/Custom Sink mode, USB + 2-Lane Custom, Orientation = Normal

Type-C Receptacle		SCHQ674401A			Sink	
Pin No.	Name	Pin	Re-routing	Pin	Function	Mode
A2, A3	TX1	URX2	←	DRX2	TX1	USB 3.x Device
B11, B10	RX1	UTX2	→	DTX2	RX1	
A11, A10	RX2	UTX1	→	DTX1	LN1	Custom
B2, B3	TX2	URX1	←	DRX1	LN0	
A8	SBU1	SBU2	←	AUXN	AUXN	
B8	SBU2	SBU1	→	AUXP	AUXP	
A5	CC1	DIR1/DIR0/CTL1/CTL0/FLIP = H/H/H/H/L				
B5	CC2					

Figure 20 1-port USB 3.2 + 2-lane Custom (Orientation : Normal to Normal)

USB/Custom Source mode, USB + 2-Lane Custom, Orientation = Flipped

Source		SCHQ674401A			Type-C Receptacle	
Mode	Function	Pin	Re-routing	Pin	Name	Pin No.
USB 3.x Host	RX2	URX2	←	DRX2	RX2	A11, A10
	TX2	UTX2	→	DTX2	TX2	B3, B2
Custom	LN1	UTX1	→	DTX1	TX1	A2, A3
	LN0	URX1	←	DRX1	RX1	B11, B10
	AUXP	AUXP	↔	SBU1	SBU1	A8
	AUXN	AUXN	↔	SBU2	SBU2	B8
DIR1/DIR0/CTL1/CTL0/FLIP = H/L/H/H/H					CC1	A5
					CC2	B5

Type-C Cable

USB/Custom Sink mode, USB + 2-Lane Custom, Orientation = Flipped

Type-C Receptacle		SCHQ674401A			Sink	
Pin No.	Name	Pin	Re-routing	Pin	Function	Mode
A2, A3	TX1	URX2	←	DRX2	LN0	Custom
B11, B10	RX1	UTX2	→	DTX2	LN1	
A11, A10	RX2	UTX1	→	DTX1	RX2	USB 3.x Device
B2, B3	TX2	URX1	←	DRX1	TX2	
A8	SBU1	SBU2	↔	AUXN	AUXN	Custom
B8	SBU2	SBU1	↔	AUXP	AUXP	
A5	CC1	DIR1/DIR0/CTL1/CTL0/FLIP = H/H/H/H/H				
B5	CC2					

Figure 21 1-port USB 3.2 + 2-lane Custom (Orientation : Flip to Flip)

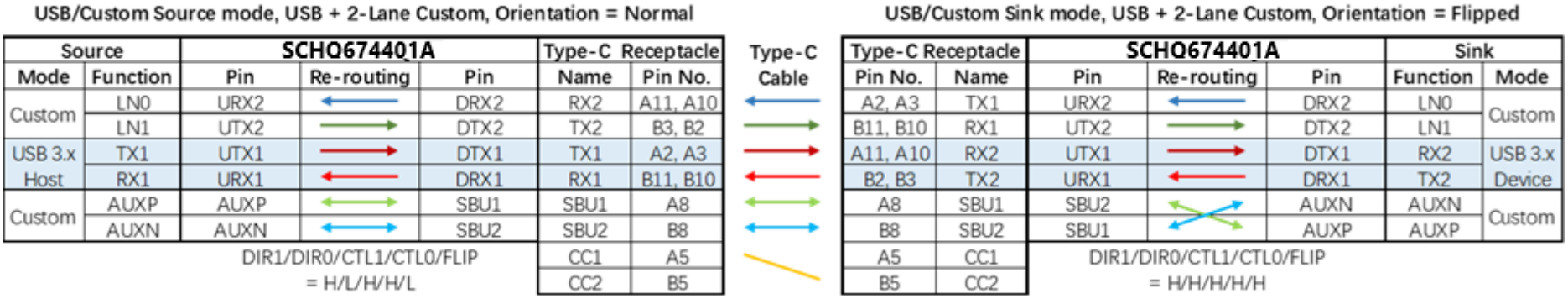


Figure 22 1-port USB 3.2 + 2-lane Custom (Orientation : Normal to Flip)

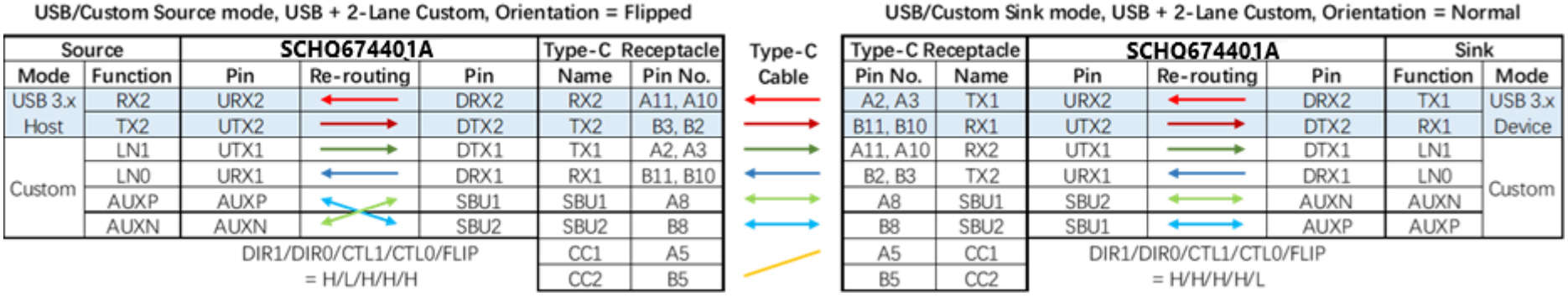


Figure 23 1-port USB 3.2 + 2-lane Custom (Orientation : Flip to Normal)

9.2.5 USB/Custom mode – 4-lane Custom

USB/Custom Source mode, 4-Lane Custom, Orientation = Normal

Source		SCHQ674401A			Type-C Receptacle	
Mode	Function	Pin	Re-routing	Pin	Name	Pin No.
Custom	LN0	URX2	←	DRX2	RX2	A11, A10
	LN1	UTX2	→	DTX2	TX2	B3, B2
	LN2	UTX1	→	DTX1	TX1	A2, A3
	LN3	URX1	←	DRX1	RX1	B11, B10
	AUXP	AUXP	→	SBU1	SBU1	A8
	AUXN	AUXN	←	SBU2	SBU2	B8
		DIR1/DIR0/CTL1/CTL0/FLIP = H/L/H/L/L			CC1	A5
					CC2	B5

Type-C Cable

USB/Custom Sink mode, 4-Lane Custom, Orientation = Normal

Type-C Receptacle		SCHQ674401A			Sink	
Pin No.	Name	Pin	Re-routing	Pin	Function	Mode
A2, A3	TX1	URX2	←	DRX2	LN3	Custom
B11, B10	RX1	UTX2	→	DTX2	LN2	
A11, A10	RX2	UTX1	→	DTX1	LN1	
B2, B3	TX2	URX1	←	DRX1	LN0	
A8	SBU1	SBU2	←	AUXN	AUXN	
B8	SBU2	SBU1	→	AUXP	AUXP	
A5	CC1	DIR1/DIR0/CTL1/CTL0/FLIP = H/H/H/L/L				
B5	CC2					

Figure 24 4-lane Custom (Orientation : Normal to Normal)

USB/Custom Source mode, 4-Lane Custom, Orientation = Flipped

Source		SCHQ674401A			Type-C Receptacle	
Mode	Function	Pin	Re-routing	Pin	Name	Pin No.
Custom	LN3	URX2	←	DRX2	RX2	A11, A10
	LN2	UTX2	→	DTX2	TX2	B3, B2
	LN1	UTX1	→	DTX1	TX1	A2, A3
	LN0	URX1	←	DRX1	RX1	B11, B10
	AUXP	AUXP	←	SBU1	SBU1	A8
	AUXN	AUXN	→	SBU2	SBU2	B8
		DIR1/DIR0/CTL1/CTL0/FLIP = H/L/H/L/H			CC1	A5
					CC2	B5

Type-C Cable

USB/Custom Sink mode, 4-Lane Custom, Orientation = Flipped

Type-C Receptacle		SCHQ674401A			Sink	
Pin No.	Name	Pin	Re-routing	Pin	Function	Mode
A2, A3	TX1	URX2	←	DRX2	LN0	Custom
B11, B10	RX1	UTX2	→	DTX2	LN1	
A11, A10	RX2	UTX1	→	DTX1	LN2	
B2, B3	TX2	URX1	←	DRX1	LN3	
A8	SBU1	SBU2	→	AUXN	AUXN	
B8	SBU2	SBU1	←	AUXP	AUXP	
A5	CC1	DIR1/DIR0/CTL1/CTL0/FLIP = H/H/H/L/H				
B5	CC2					

Figure 25 4-lane Custom (Orientation : Flip to Flip)

USB/Custom Source mode, 4-Lane Custom, Orientation = Normal

Source		SCHQ674401A			Type-C Receptacle	
Mode	Function	Pin	Re-routing	Pin	Name	Pin No.
Custom	LN0	URX2	←	DRX2	RX2	A11, A10
	LN1	UTX2	→	DTX2	TX2	B3, B2
	LN2	UTX1	→	DTX1	TX1	A2, A3
	LN3	URX1	←	DRX1	RX1	B11, B10
	AUXP	AUXP	→	SBU1	SBU1	A8
	AUXN	AUXN	→	SBU2	SBU2	B8
		DIR1/DIR0/CTL1/CTL0/FLIP = H/L/H/L/L			CC1	A5
					CC2	B5

Type-C Cable

USB/Custom Sink mode, 4-Lane Custom, Orientation = Flipped

Type-C Receptacle		SCHQ674401A			Sink	
Pin No.	Name	Pin	Re-routing	Pin	Function	Mode
A2, A3	TX1	URX2	←	DRX2	LN0	Custom
B11, B10	RX1	UTX2	→	DTX2	LN1	
A11, A10	RX2	UTX1	→	DTX1	LN2	
B2, B3	TX2	URX1	←	DRX1	LN3	
A8	SBU1	SBU2	⇄	AUXN	AUXN	
B8	SBU2	SBU1	⇄	AUXP	AUXP	
A5	CC1	DIR1/DIR0/CTL1/CTL0/FLIP = H/H/H/L/H				
B5	CC2					

Figure 26 4-lane Custom (Orientation : Normal to Flip)

USB/Custom Source mode, 4-Lane Custom, Orientation = Flipped

Source		SCHQ674401A			Type-C Receptacle	
Mode	Function	Pin	Re-routing	Pin	Name	Pin No.
Custom	LN3	URX2	←	DRX2	RX2	A11, A10
	LN2	UTX2	→	DTX2	TX2	B3, B2
	LN1	UTX1	→	DTX1	TX1	A2, A3
	LN0	URX1	←	DRX1	RX1	B11, B10
	AUXP	AUXP	⇄	SBU1	SBU1	A8
	AUXN	AUXN	⇄	SBU2	SBU2	B8
		DIR1/DIR0/CTL1/CTL0/FLIP = H/L/H/L/H			CC1	A5
					CC2	B5

Type-C Cable

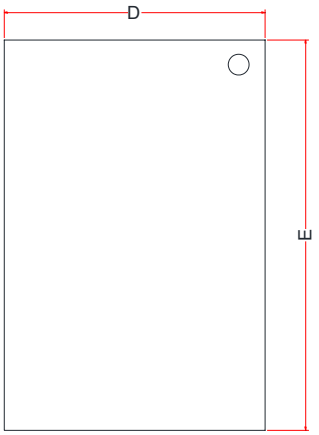
USB/Custom Sink mode, 4-Lane Custom, Orientation = Normal

Type-C Receptacle		SCHQ674401A			Sink	
Pin No.	Name	Pin	Re-routing	Pin	Function	Mode
A2, A3	TX1	URX2	←	DRX2	LN3	Custom
B11, B10	RX1	UTX2	→	DTX2	LN2	
A11, A10	RX2	UTX1	→	DTX1	LN1	
B2, B3	TX2	URX1	←	DRX1	LN0	
A8	SBU1	SBU2	→	AUXN	AUXN	
B8	SBU2	SBU1	→	AUXP	AUXP	
A5	CC1	DIR1/DIR0/CTL1/CTL0/FLIP = H/H/H/L/L				
B5	CC2					

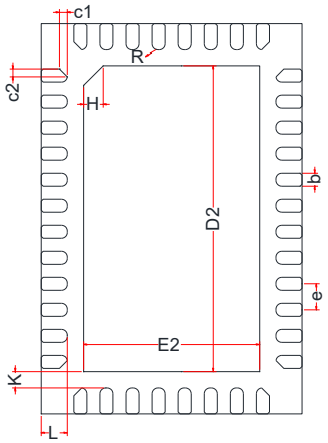
Figure 27 4-lane Custom (Orientation : Flip to Normal)

10 Package Outline Dimensions

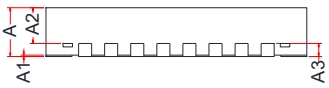
QFN4x6-40L



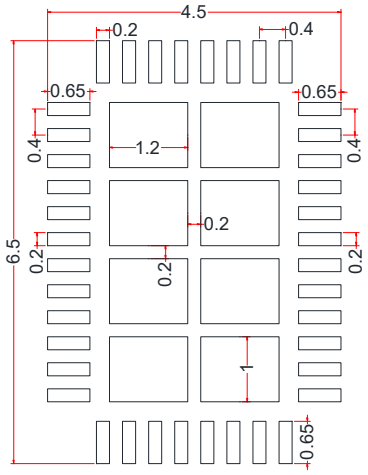
TOP VIEW



BOTTOM VIEW



SIDE VIEW

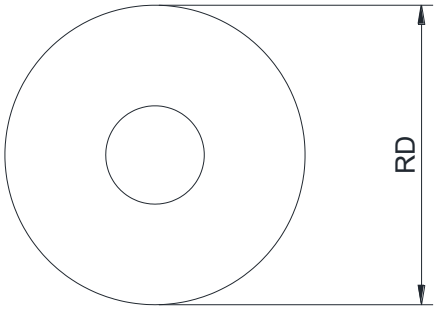


RECOMMENDED LAND PATTERN(Unit:mm)

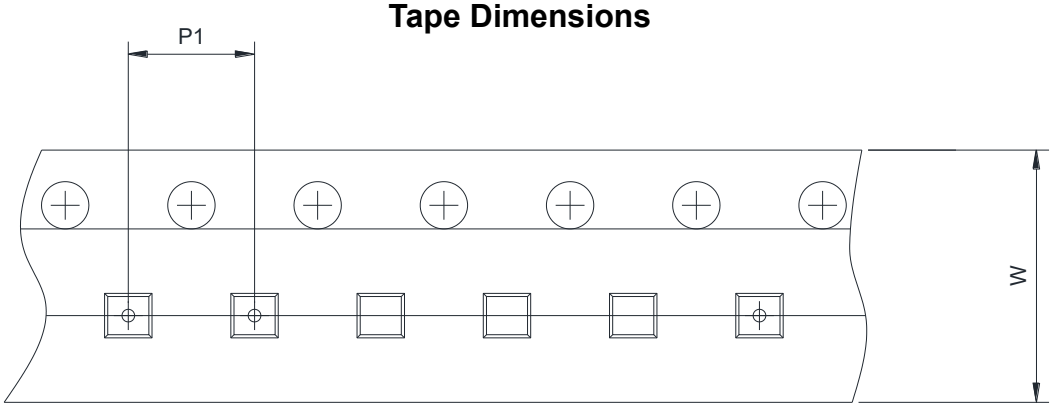
Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.40	0.55	0.60
A3		0.20REF	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	5.90	6.00	6.10
D2	4.60	4.70	4.80
E2	2.60	2.70	2.80
e		0.40 BSC	
H		0.30 REF	
K	0.15	0.25	0.35
L	0.35	0.40	0.45
R	0.09	-	-
c1/c2	-	0.12	-

11 Tape And Reel Information

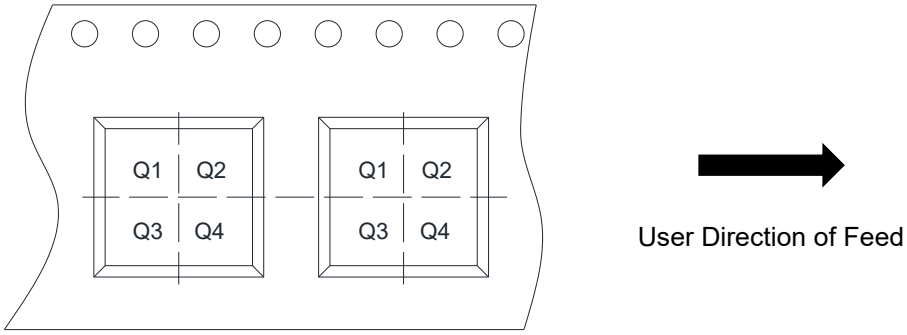
Reel Dimensions



Tape Dimensions



Quadrant Assignments for PIN1 Orientation in Tape



RD	Reel Dimension	☐ 7inch	☑ 13inch		
W	Overall width of the carrier tape	☐ 8mm	☑ 12mm	☐ 16mm	
P1	Pitch between successive cavity centers	☐ 2mm	☐ 4mm	☑ 8mm	
Pin1	Pin1 Quadrant	☐ Q1	☑ Q2	☐ Q3	☐ Q4